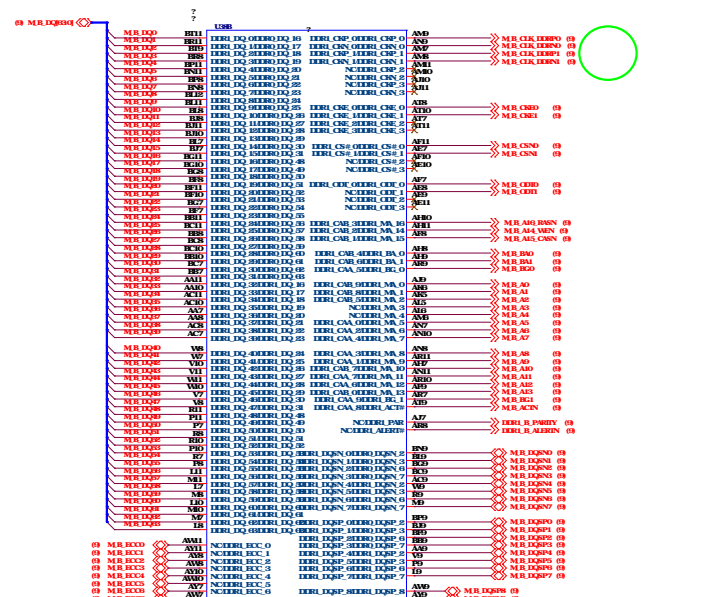
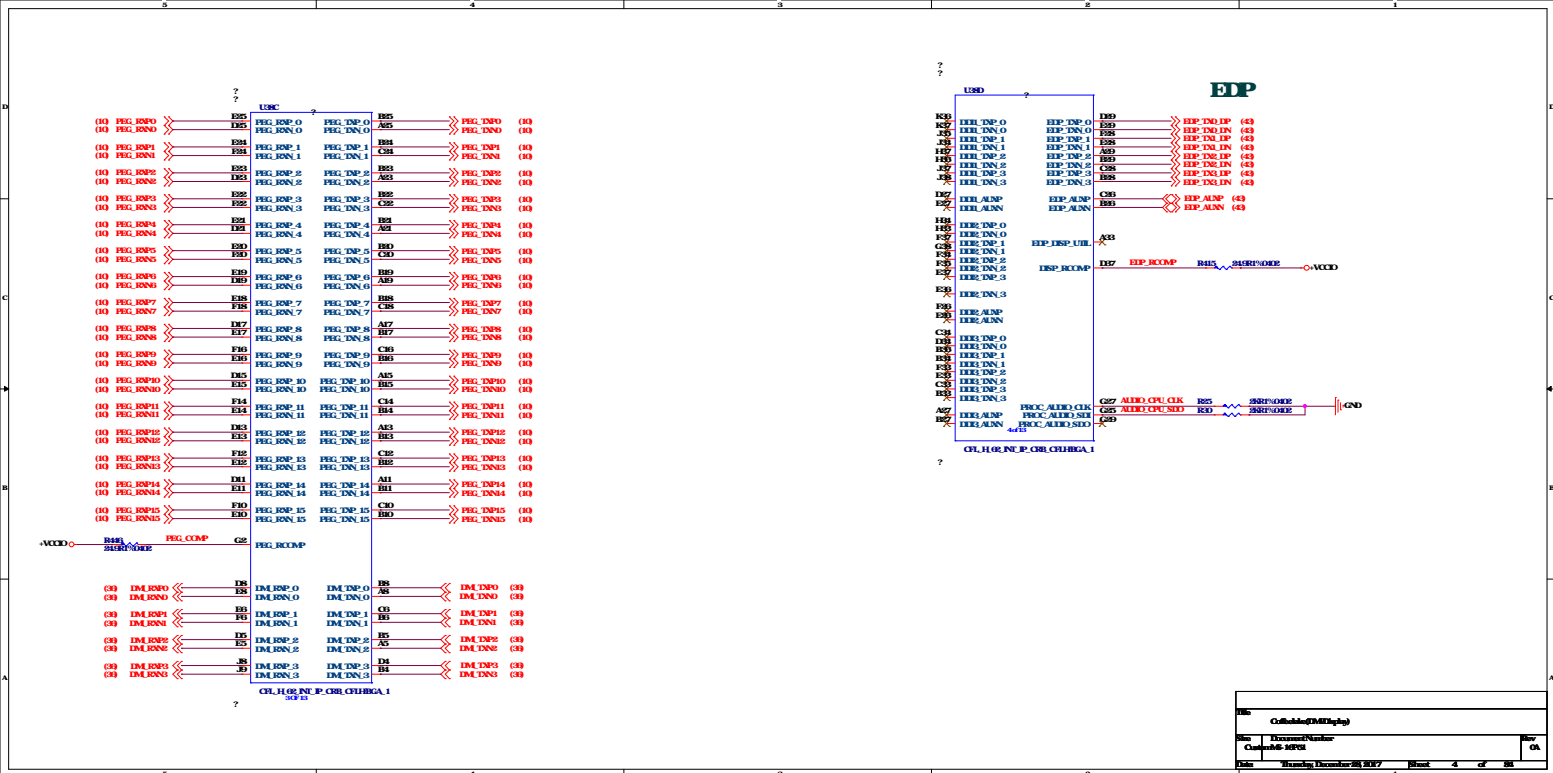


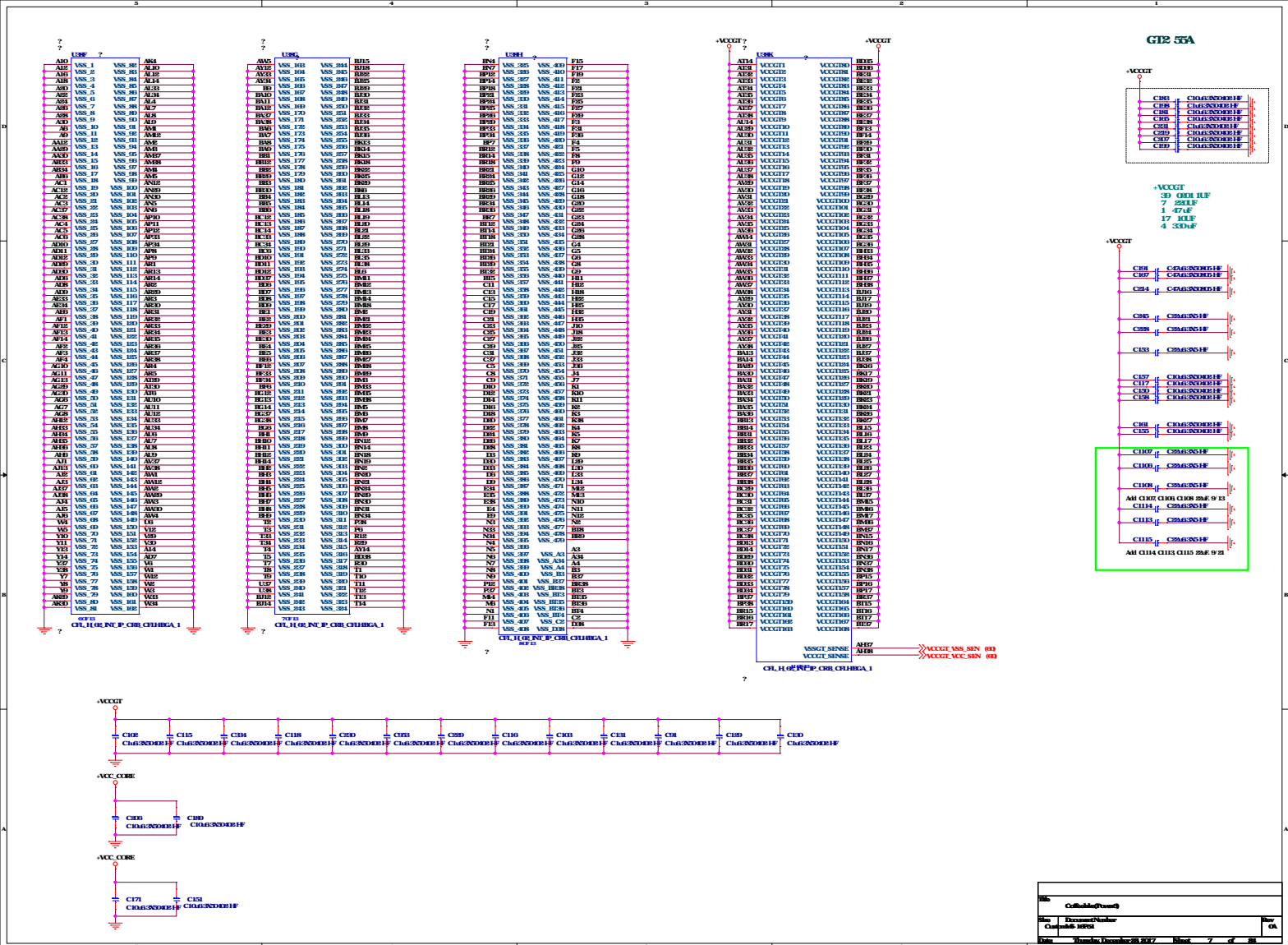
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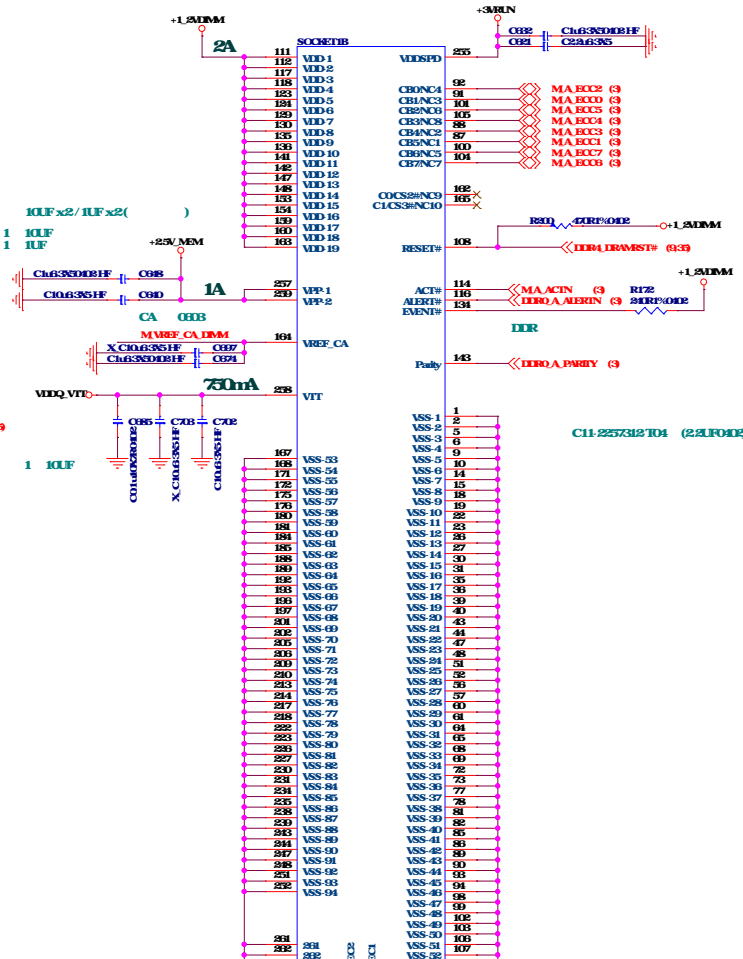


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CAS#			Rev
Cellulose 10000			01
Date	Sunday, December 08, 2019		Print
1		2	3 of 34



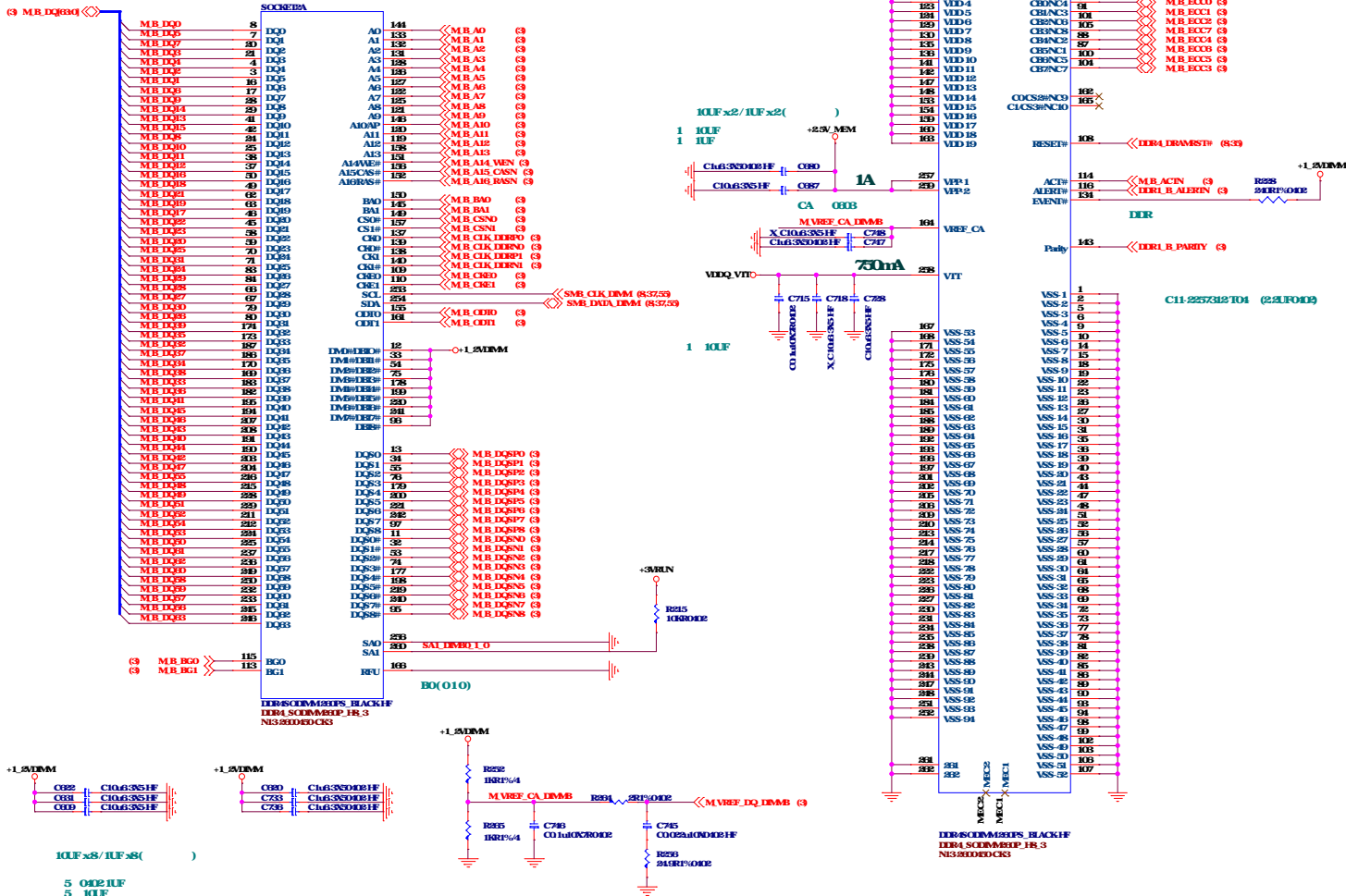
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Site Cust	Document Number Cust# 48- 86708			Rev CA
Date	Thursday, December 28, 2006		Sheet	5 of 28





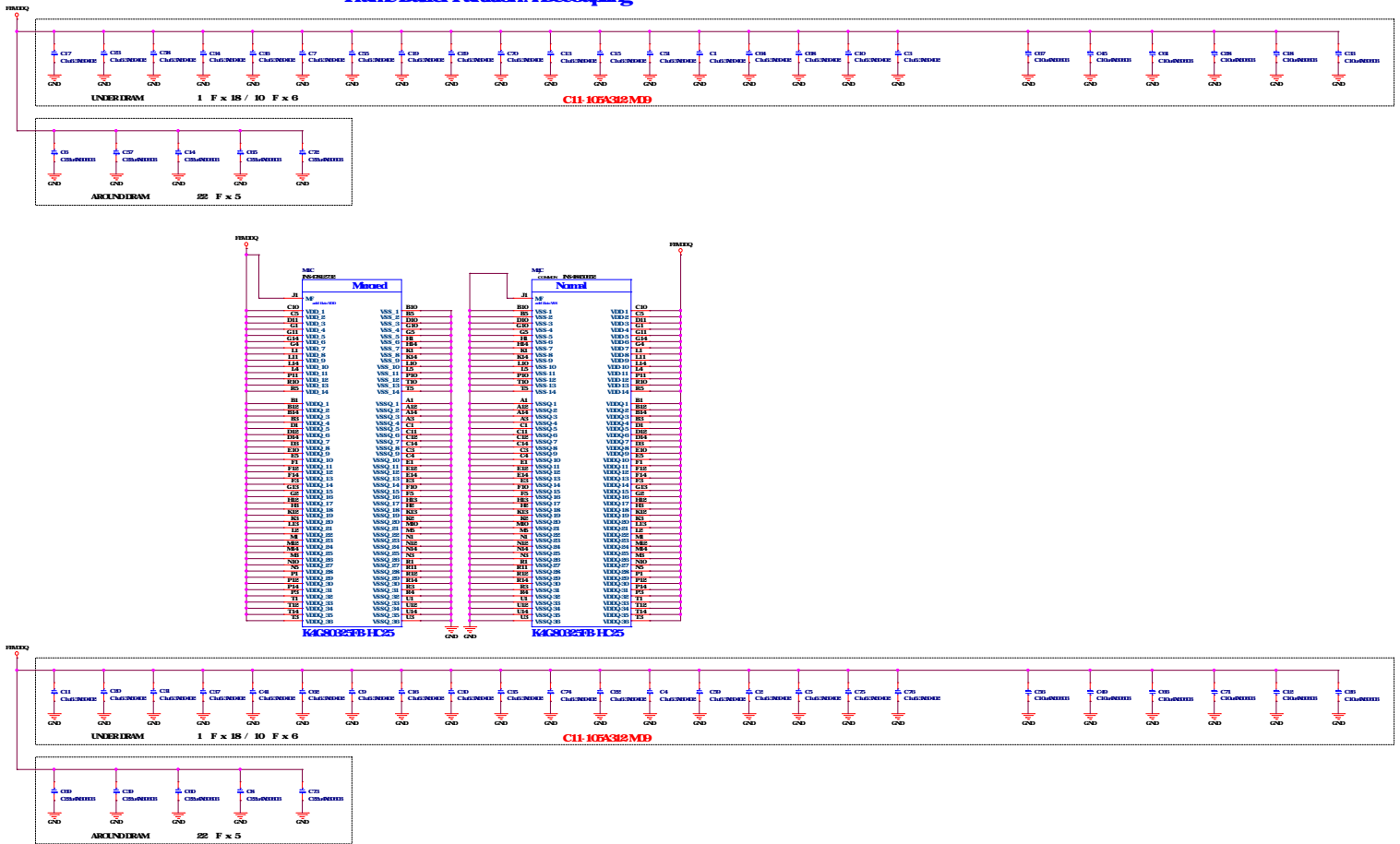
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DDA, SCORP/40				
Site Customer	Document Number MFCR			Rev CA
Date	Tracking December 28, 2017		Sheet	8 of 88

SODIMM_B0(TOP-Reverse)

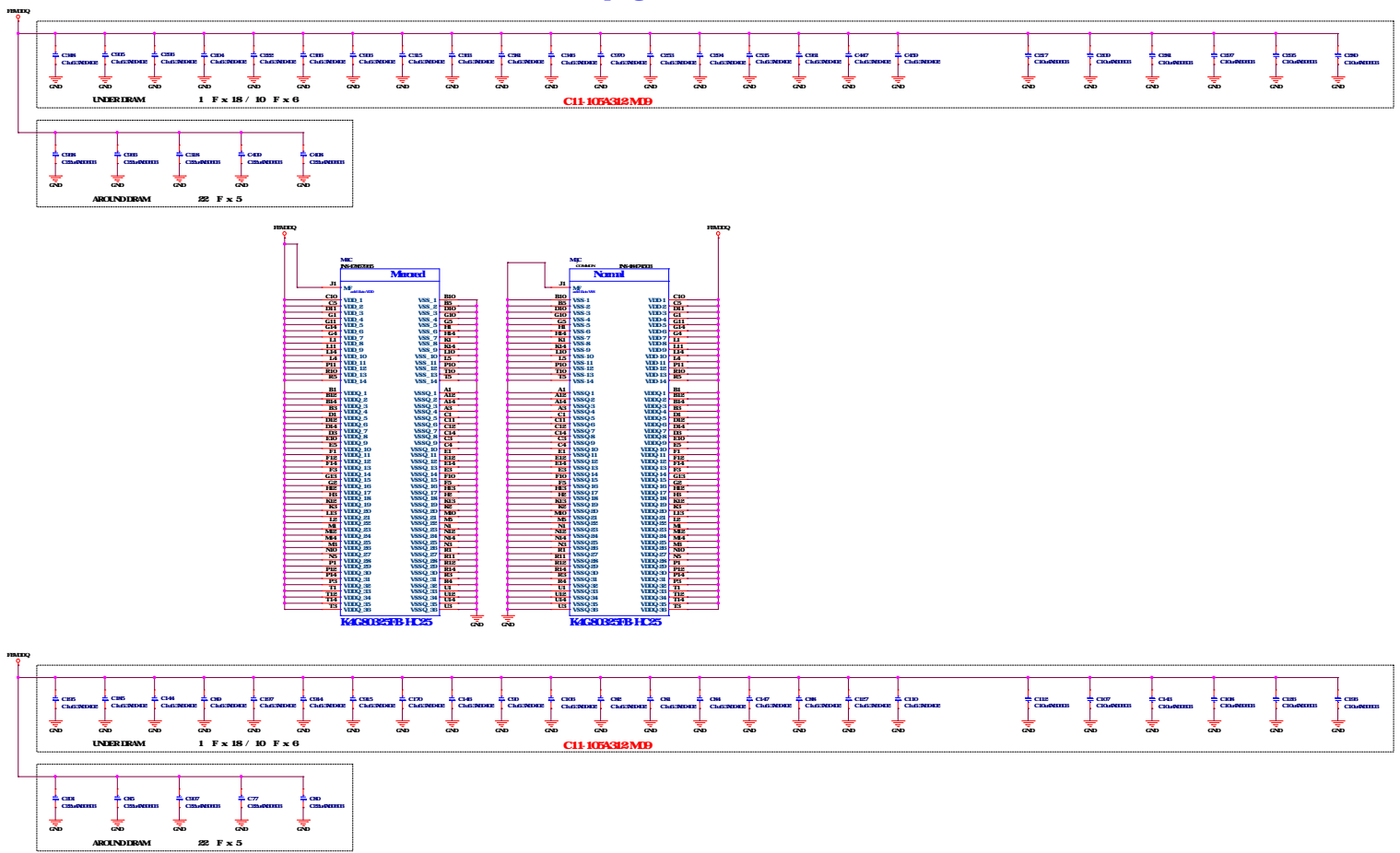


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Rev	Document Number	Rev	CA
CA	00000000		
Date	Thursday, December 28, 2017	Sheet	9 of 24

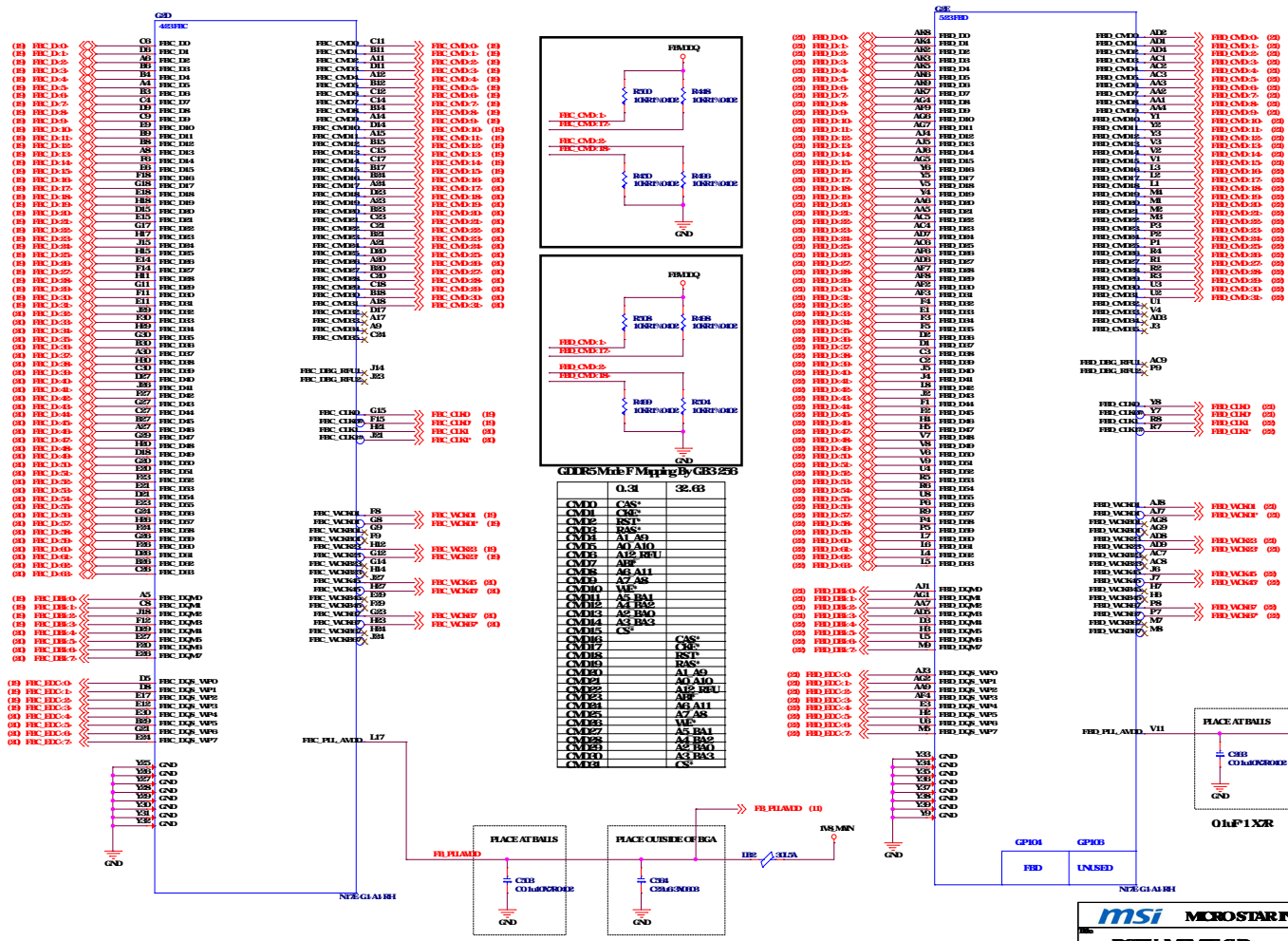
Frame Buffer Partition A Decoupling



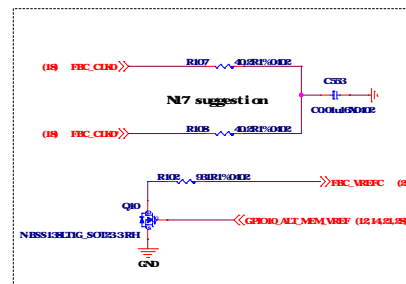
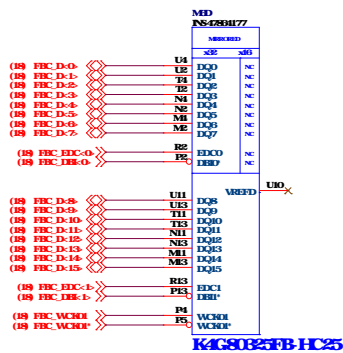
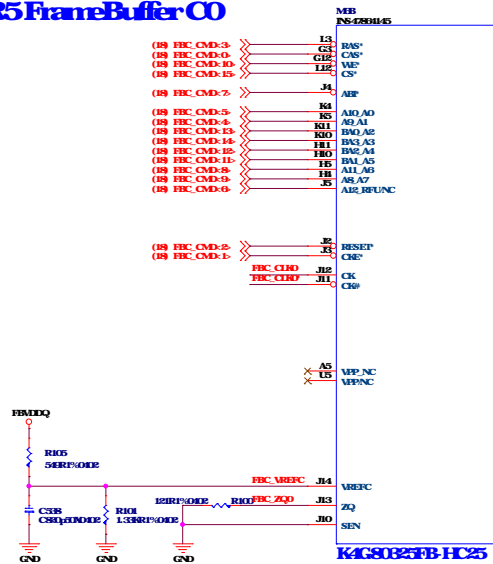
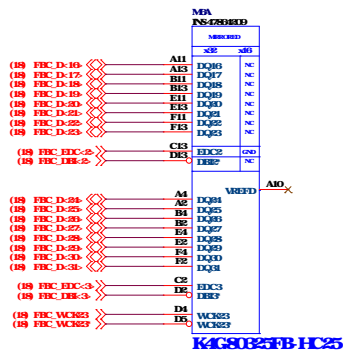
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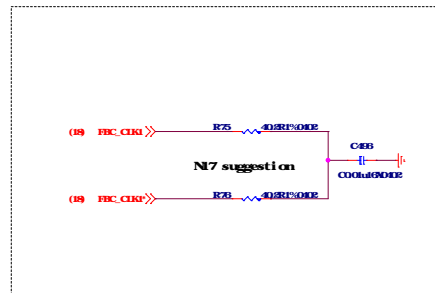
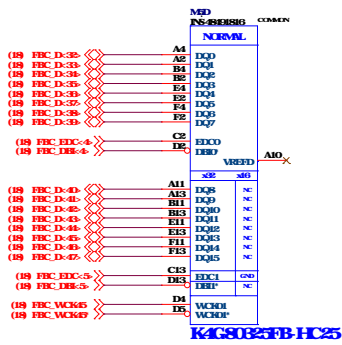
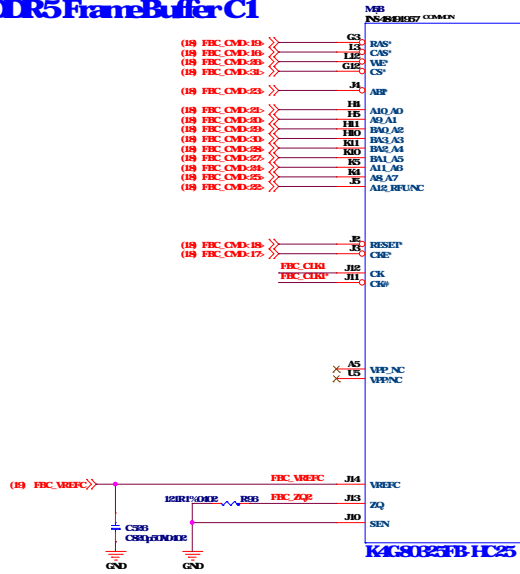
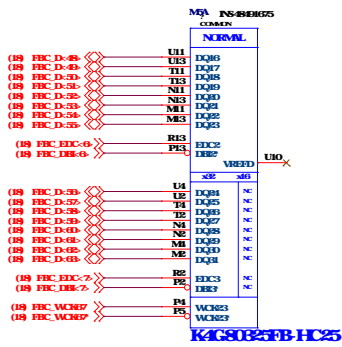
GPU Frame Buffer Partition C/D



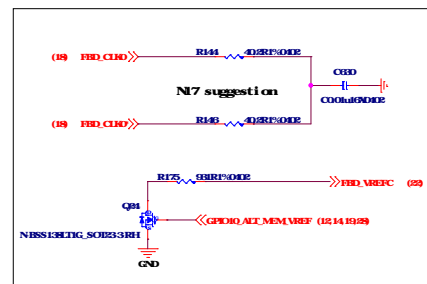
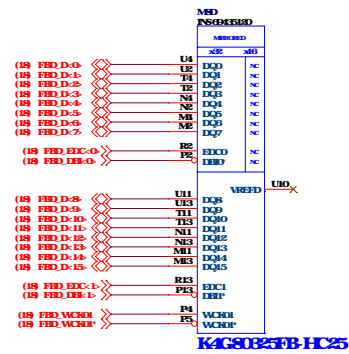
DGPU_GDDR5FrameBufferC0



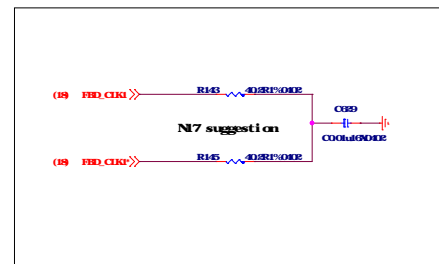
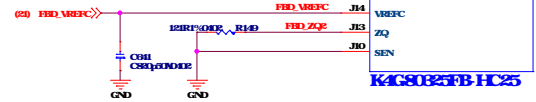
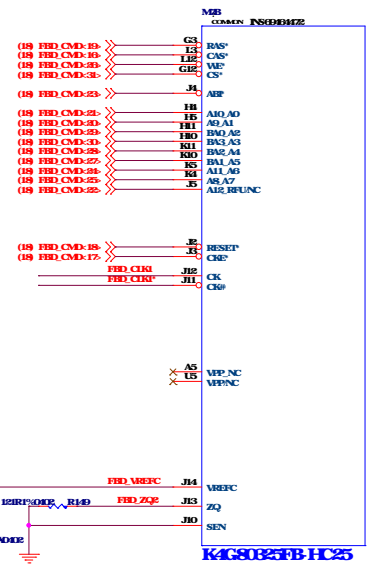
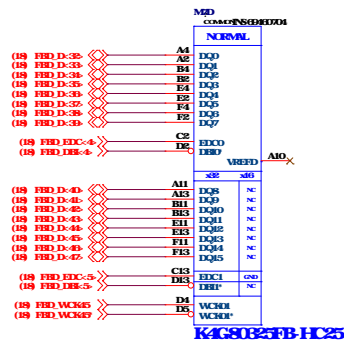
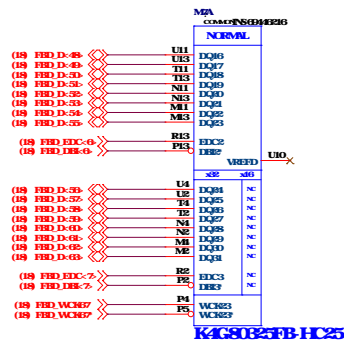
DGPU_GDDR5FrameBufferC1



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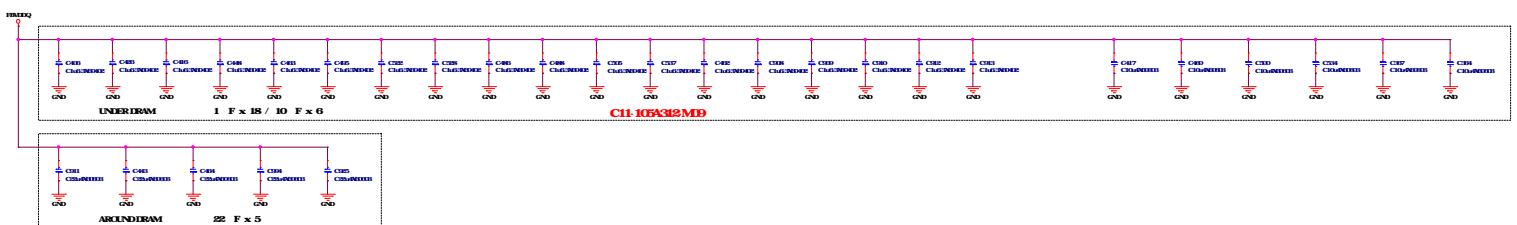
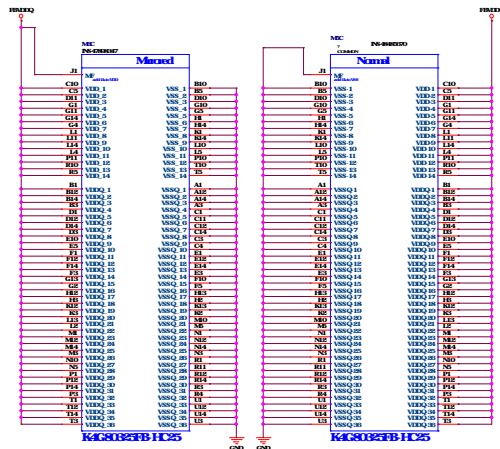
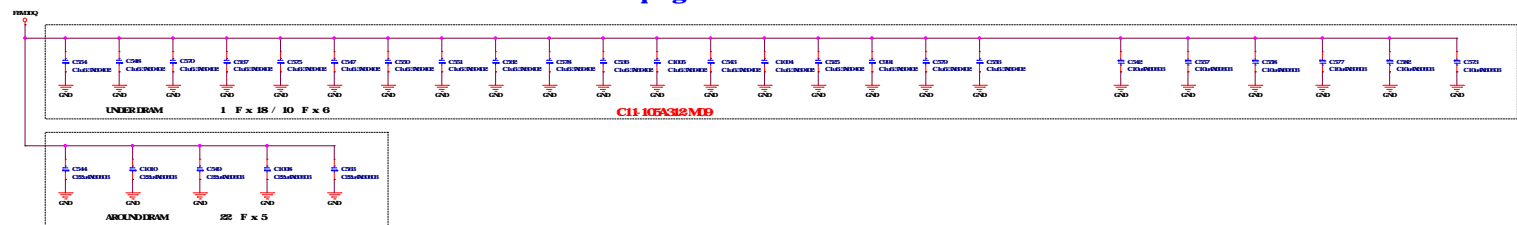


Title			
DGFU GUIDES Manual for ID			
Size A3	Document Number MS-18FC1		Rev 0A
Date	Issued		of
	December 26, 2017		28

DGPU_GDDR5FrameBufferD1

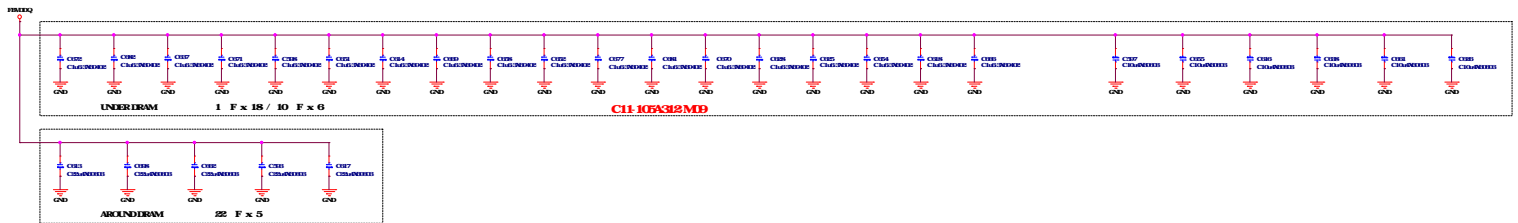
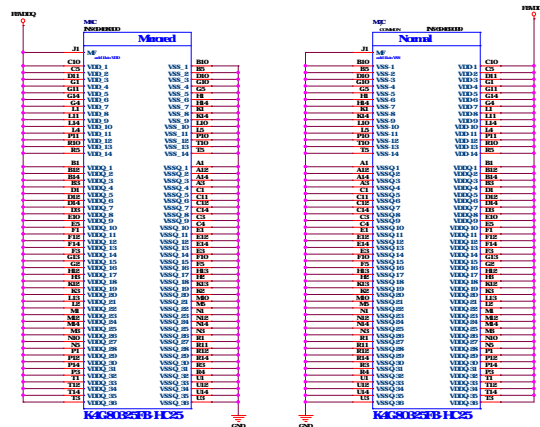
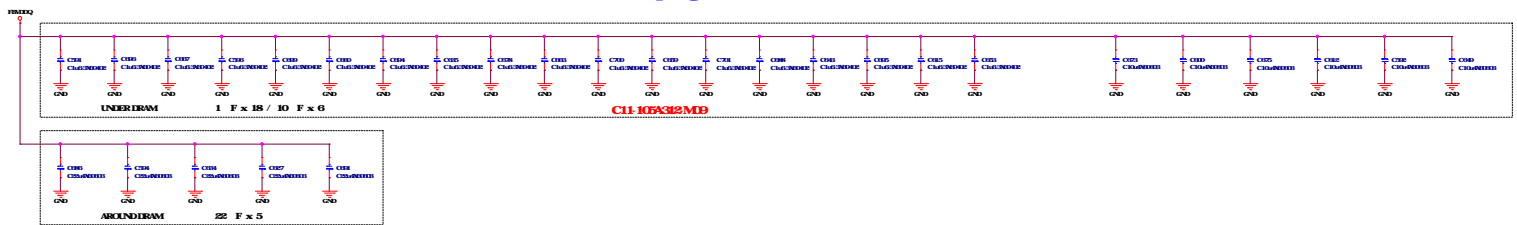
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ICRU CODES Form 8-10			
Site	Document Number		Site
AS	MS-18081		CA
Date	Transcribing Date	Sheet	of
	Thursday, December 23, 2017	22	24

Frame Buffer Partition C Decoupling



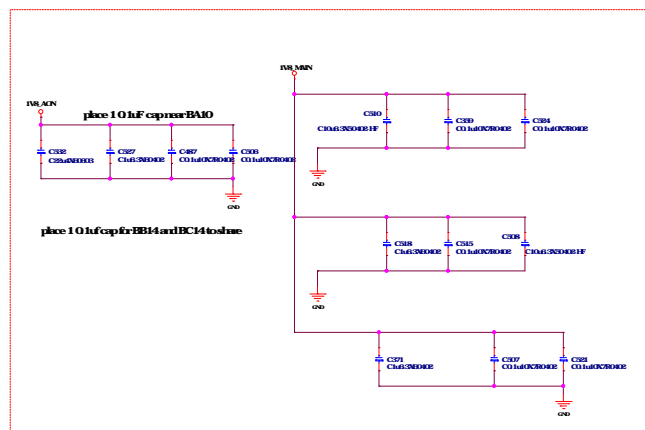
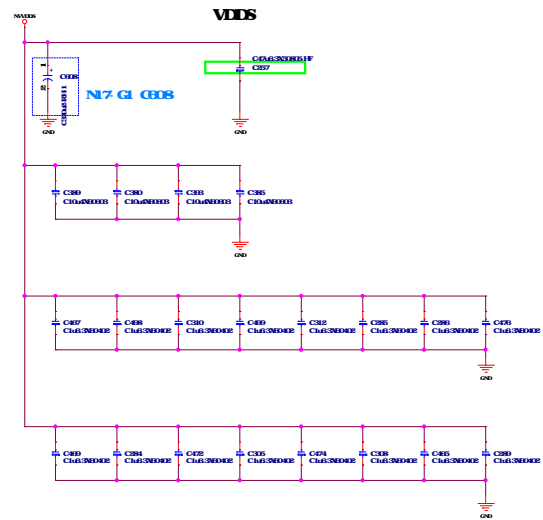
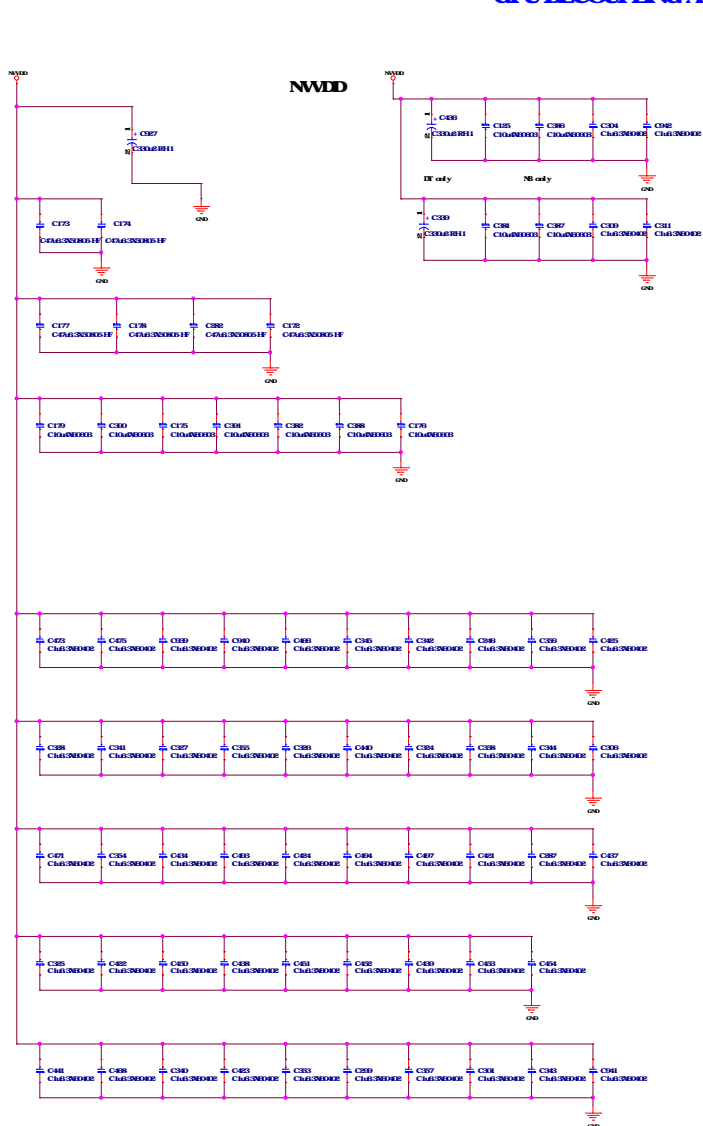
Micron PN: M12250225 M30 / M12L250M32 F-80A (250Mx32bit)
Samsung PN: M12803235 S02 / K6G832FB-HC25 (250Mx32bit)

Frame Buffer Partition D Decoupling



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GPU DECOUPLING A



GPU DECOUPLING B

FBVDDQ

FBVDDQ

Partition A

2X10U, 6X1U

Partition B

2X10U, 6X1U

Partition C

2X10U, 6X1U

Partition D

2X10U, 6X1U

Place close to GPU

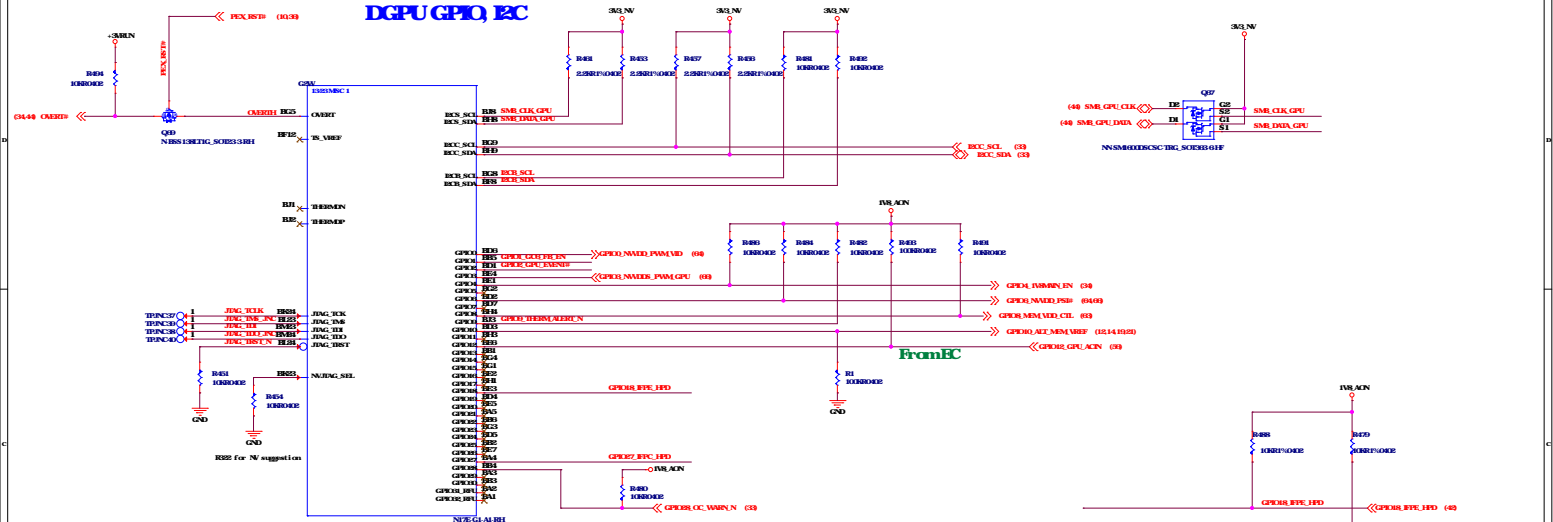
4X1U

Place close to GPU

0x8U

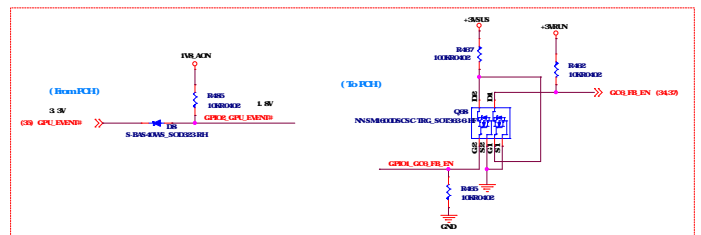
msi MICRO-STAR INT'L CO., LTD.	
DGPU GPU DECOUPLING B	
Doc. No.	Doc. Number
MS-16P51	MS-16P51
Date	Version
2018.12.07	1.00

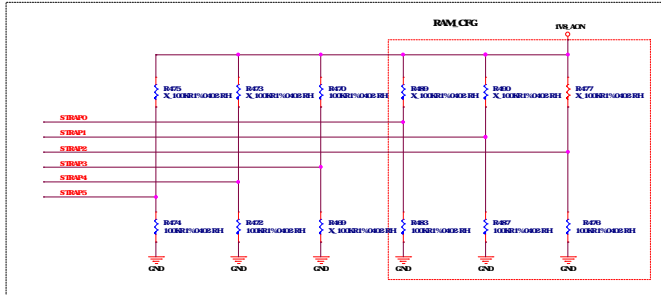
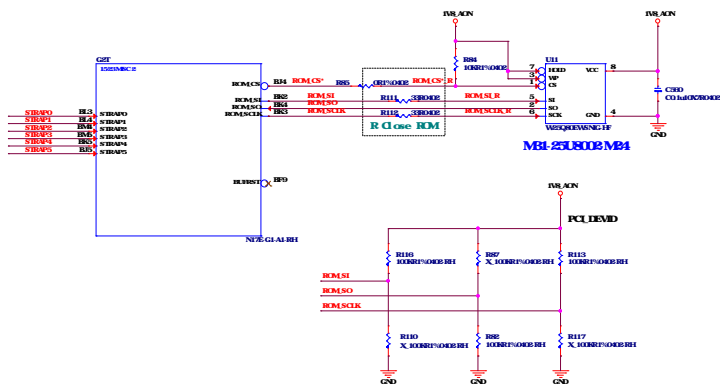
DGPU GPIO EC



Vinafix

Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWM_VID	O	GPU Gate VID PWM control signal	0 to V8 PWM output
GPIO1	GPU_FB_EN	O	FB Enable for G3 & 1	10K pull-down
GPIO2	GPU_ENABLE	I	GPU enable signal for G3 & 1	10K pull-up to V8_AON
GPIO3	NAVD_SRM/PWM	O	PWM output to control the SRM power supply	10K pull-up to V8_AON
GPIO4	FB_MEN_EN	O	GPU FBMR Sequencing for G3 & 1	10K pull-up to V8_AON
GPIO5	FB_MCLK	I	Active Low FBMR Clock	10K pull-up to V8_AON
GPIO6	PSI	O	Power Sequencing	10K pull-up to V8_AON
GPIO7	LOD_H_PWM	O	Panel Backlight PWM/Brightness Control	10K pull-down
GPIO8	MEM_VREF_CTL	O	Memory Voltage Control	pull-up/pull-down to set the memory voltage on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	10K pull-down
GPIO11	LOD_VCC	O	Panel Power Enable	10K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	10K pull-up to V8_AON
GPIO13	LOD_BEN	O	Panel Backlight Enable	10K pull-down
GPIO14	HPO_A	I	Hot Plug Detect for HPPA	
GPIO15	HPO_B	I	Hot Plug Detect for HPPB	
GPIO16	SYS_RESET_MONF	I	System side PCI reset Monitor	10K pull-up to 3V3_AON
GPIO17	HPO_D	I	Hot Plug Detect for HPPD	
GPIO18	HPO_E	I	Hot Plug Detect for HPPF	
GPIO19	3D_Motion	O	3D Motion L/R signal	10K pull-down
GPIO20	NAVD_PSI	O	3D Motion L/R signal	
GPIO21	SLI_MASTER_SYNC	I	SLI Master Sync	10K pull-down
GPIO22	SLI_SWAP_RDY	I	SLI Swap Ready	1K pull-up to 3V3_AON
GPIO23	GPU_RESET_HOLD	O	GPU PCIe self-reset control	10K pull-up to 3V3
GPIO24	HPO_F	I	Hot Plug Detect for HPPF	
GPIO25	RESERVED			
GPIO26	RESERVED			
GPIO27	HPO_C	I	Hot Plug Detect for HPPC	
GPIO28	OC_WARN	I	Over current thresholding	10K pull-up to V8_AON
GPIO29	FBM_CURRENT	I	Input from power supply	0 to V8
GPIO30	RESERVED			





<p>DEFAULT SETTING</p> <p><input type="checkbox"/> V.0001</p> <p>MIS 803235 SQE</p> <p>X JG680323FB HC25</p>	<p>V.0001</p> <p>5010</p>
<p><input type="checkbox"/> V.0001</p> <p>MIS 803325 MED</p> <p>X MISLE803325F-80A</p>	<p>V.0001</p> <p>5010</p>
<p><input type="checkbox"/> V.0001</p> <p>MIS 50C23405 HES</p> <p>X FHGC23405ER TIC</p>	<p>V.0001</p> <p>5010</p>

STRAP2	STRAP1	STRAP0	RAMCFG[40]
L	L	L	0000
L	L	H	0001
L	H	L	0010
L	H	H	0011
H	H	L	0110
H	H	H	0111

H=High /Tied to L8V
M=Middle/Tied to 09V
L=Low /Tied to 0V

SAMSUNG OND
MICRON ON1
HYNIX ON2

ROM/ISO	ROM/MSI	ROM/SCLK	SCR_ENPOSED[3]	LEN/ABLE_OEN/ABLE
L	L	L	1111 DEFAULT	SCRD12/3/EN/ABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

STRAP3	STRAP4	STRAP5	SMPLA1_ADDR	DEVRSEL	POE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1DEFMLET
L	L	L	0	0	0	0 V

```

1:SMR_ALT_ADDR ENABLE
QSMR_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
QDEVID_SEL ORIGINAL

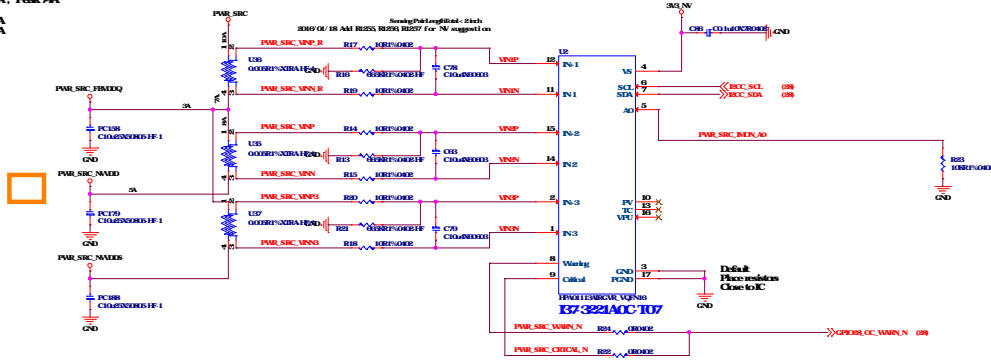
1:PCIE_CFG LOWPOWER
QPCIE_CFG HIGHPOWER

1:VGA_DEVICE ENABLE
QVGA_DEVICE DISABLE

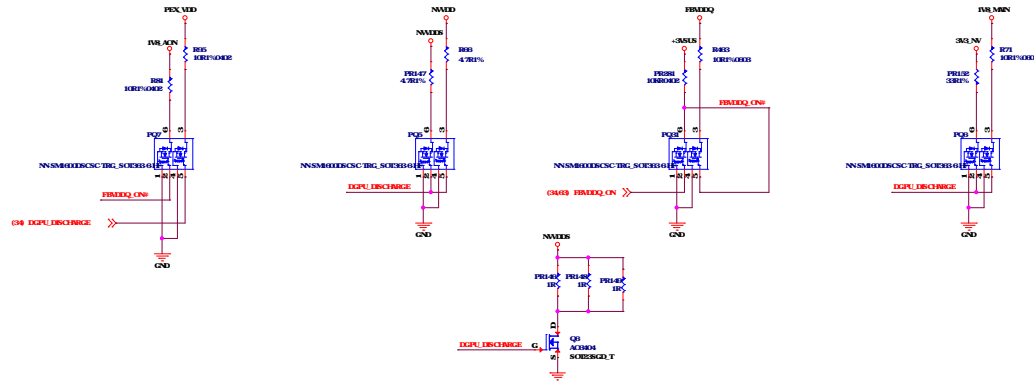
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DGPU_PowerControl

EDP Design Guide
 N17E G180M
 NVAID: 58A: Peak 1.58A
 NVAID: 58A: Peak 70A
 1.58V: 0.5A
 PEK_VDD: 3A
 PEK_VDD: 3A

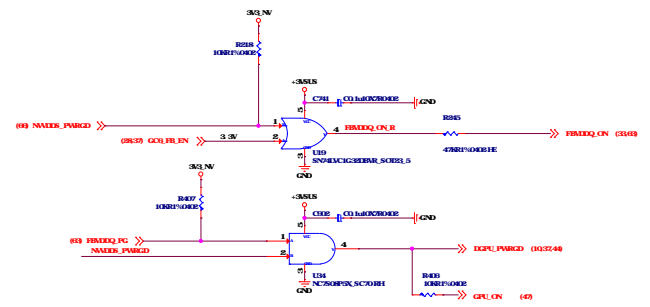
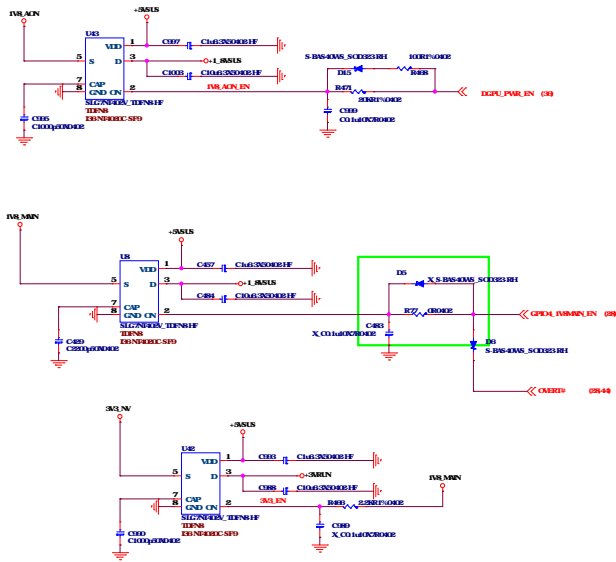


Discharge



nVIDIA Power Sequence Power UP

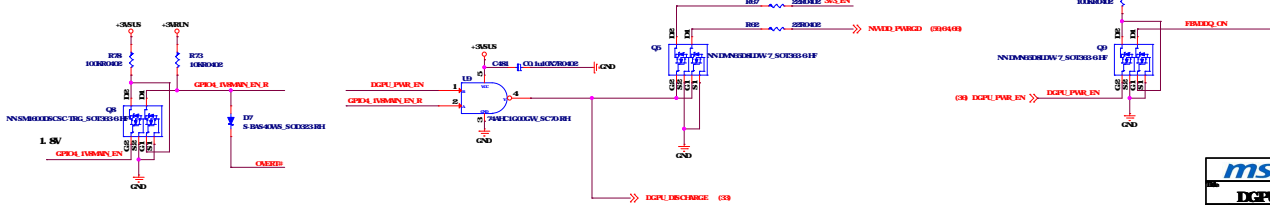
Power on= IVS_AON-> IVS_MAIN-> 3V3_NV-> NVDD-> NVDS/PEX_VDD-> FBVDDQ-> DGPUPWRGD

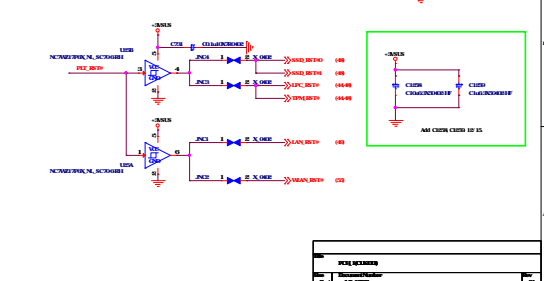
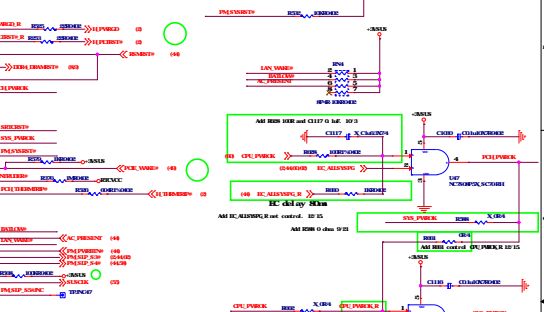
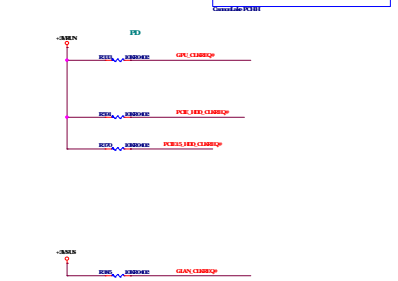
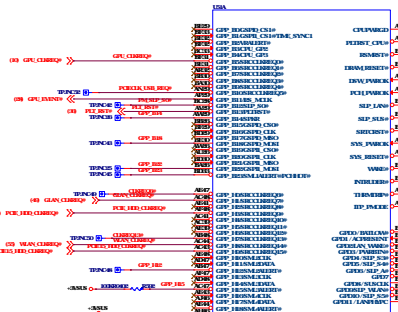
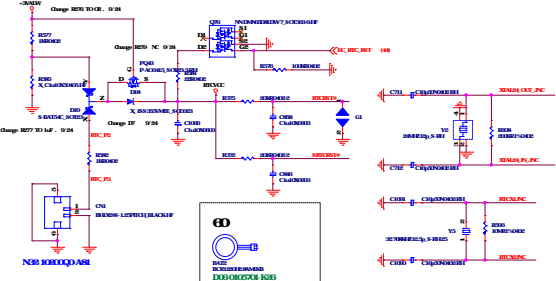
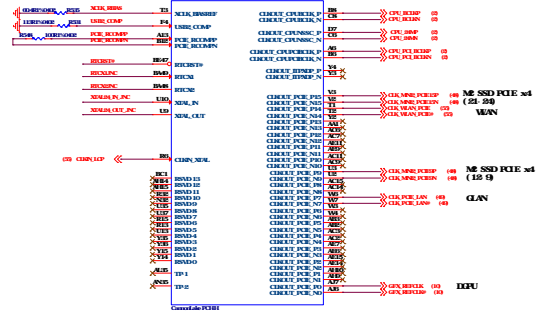


nVIDIA Power Sequence Power Down

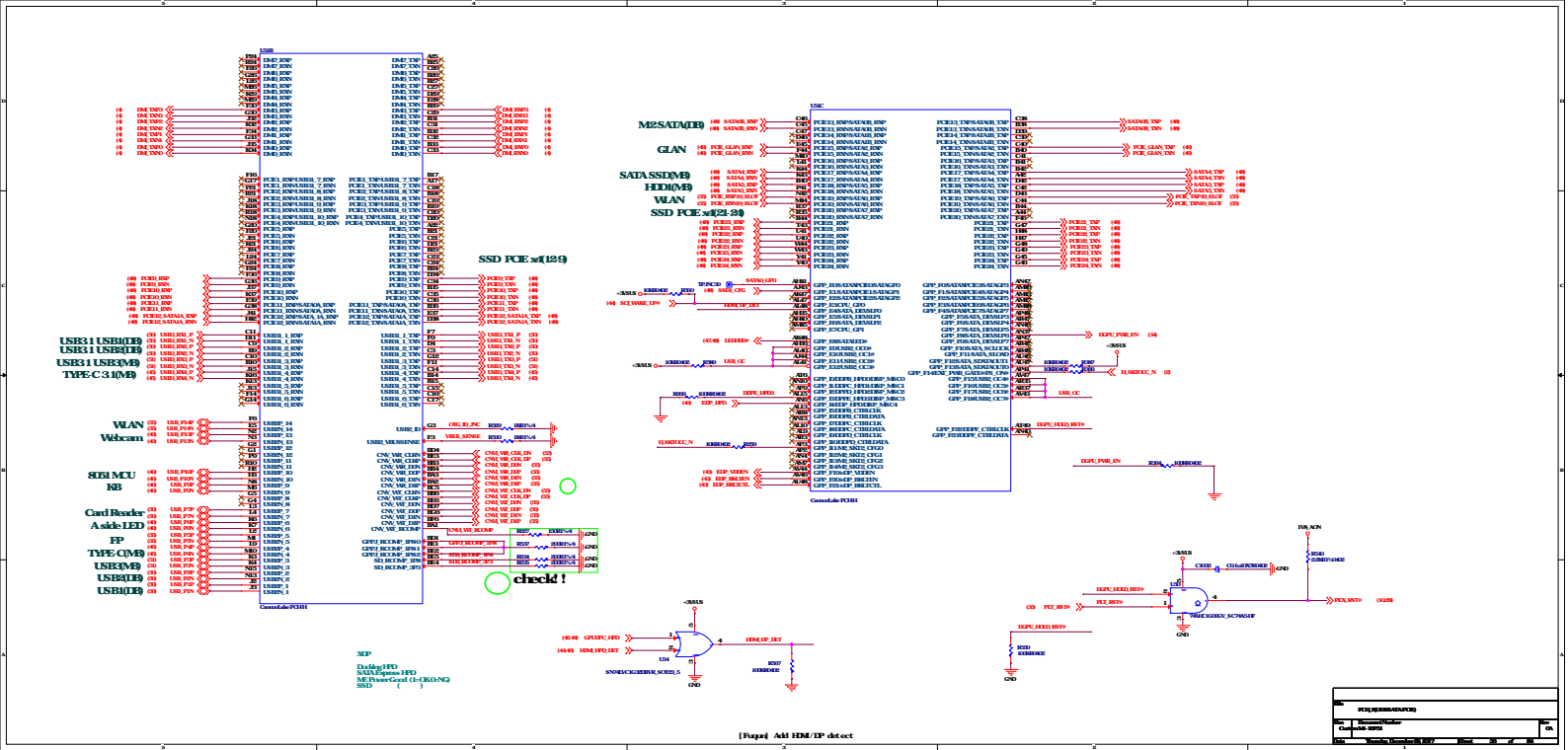
Power down= FBVDDQ-> NVDS/PEX_VDD-> 3V3_NV-> IVS_AON-> IVS_MAIN

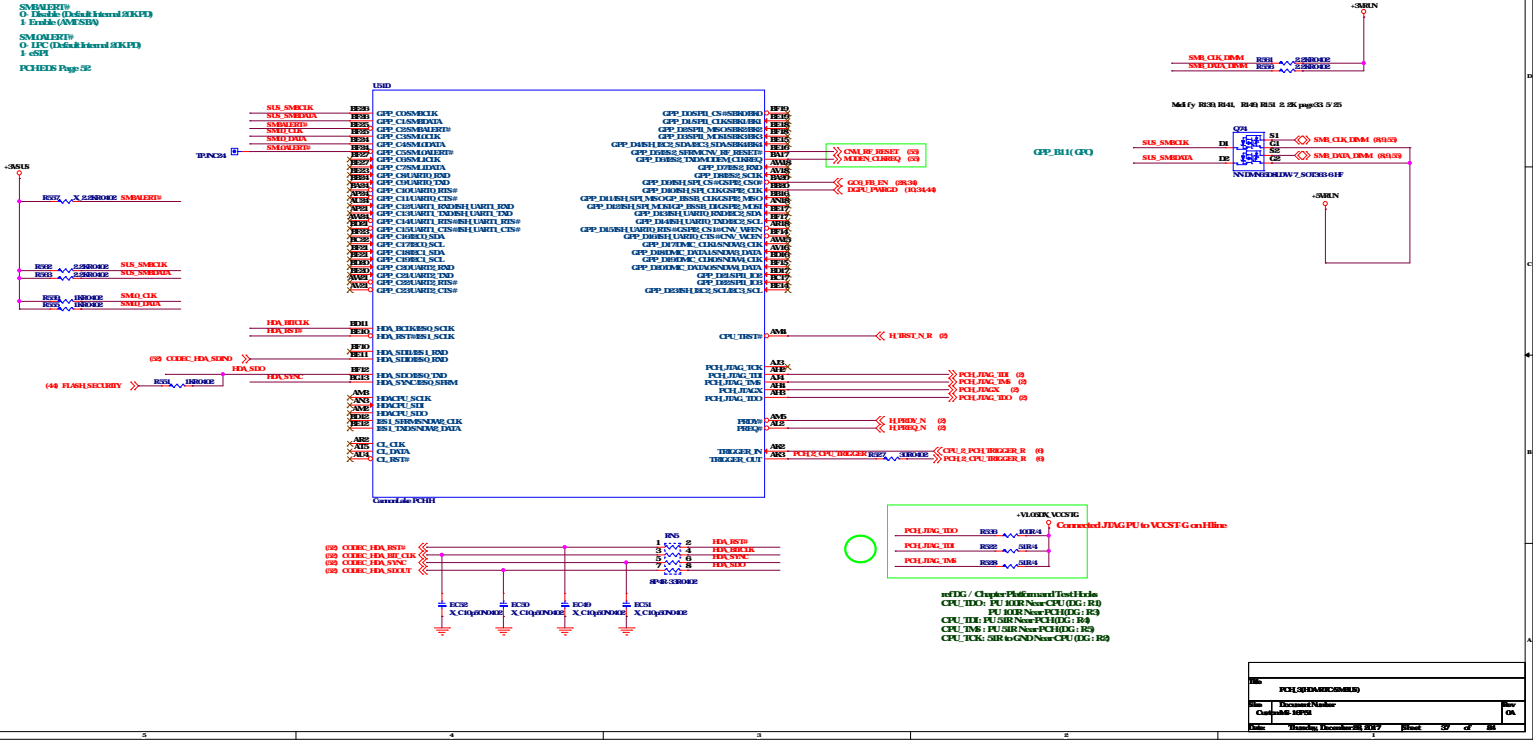
Q2/Q3 Q4 charge to D3 GDS10 D07



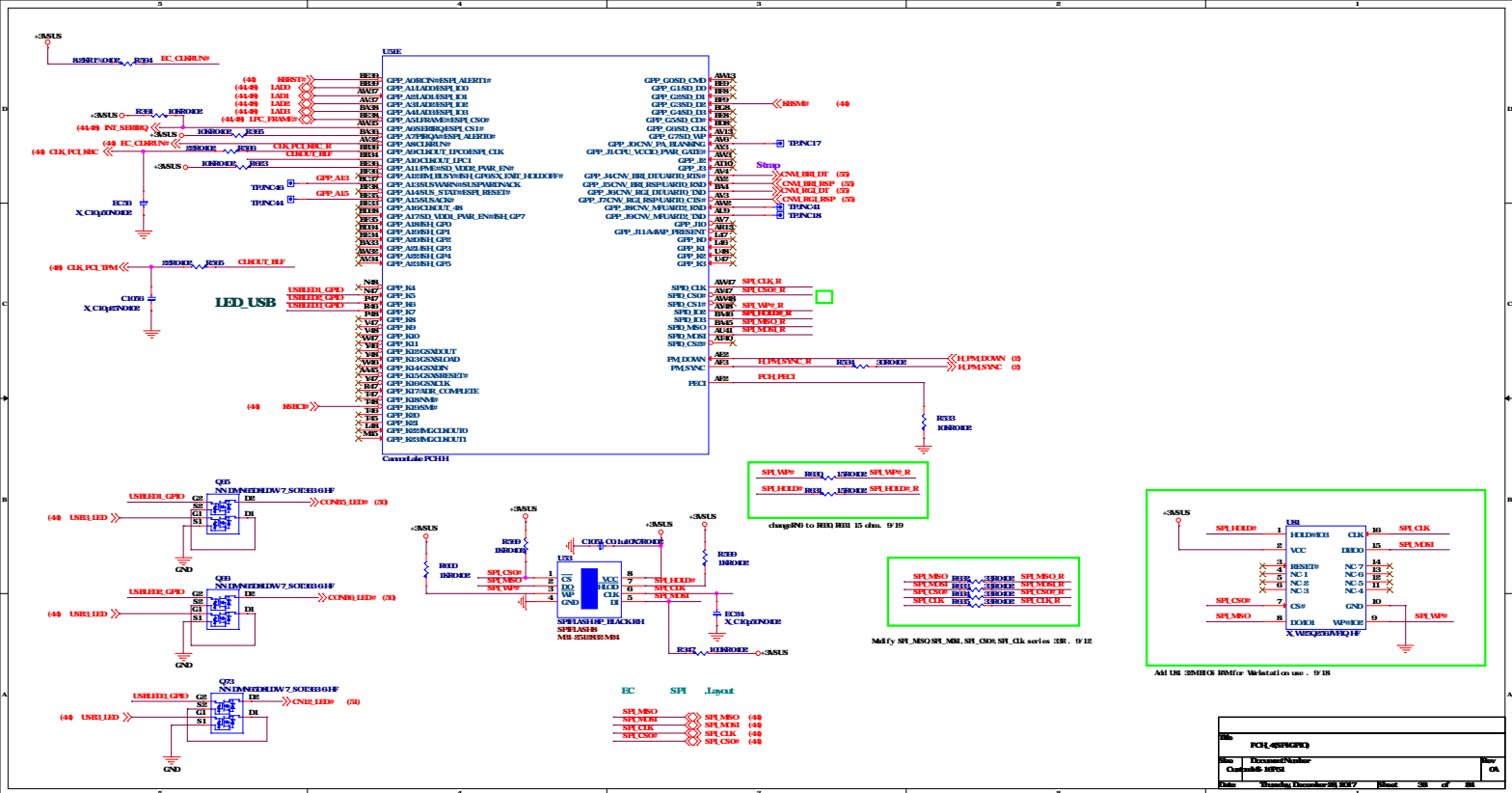


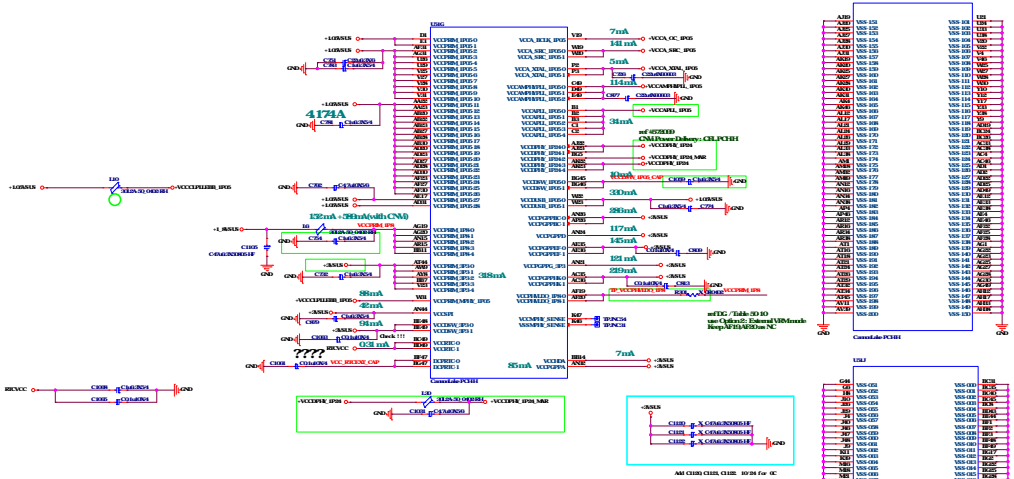
Item	Description	Value
1	ME SSD PCIe x4 (15 G)	15 G
2	ME SSD PCIe x4 (15 G)	15 G
3	ME SSD PCIe x4 (15 G)	15 G
4	ME SSD PCIe x4 (15 G)	15 G
5	ME SSD PCIe x4 (15 G)	15 G
6	ME SSD PCIe x4 (15 G)	15 G
7	ME SSD PCIe x4 (15 G)	15 G
8	ME SSD PCIe x4 (15 G)	15 G
9	ME SSD PCIe x4 (15 G)	15 G
10	ME SSD PCIe x4 (15 G)	15 G





PCH/HS (Platform Controller Hub)			
Rev	1.0	Rev	1.0
Author	Intel	Rev	1.0
Checklist	Intel	Rev	1.0
Date	Thursday, December 28, 2017	Sheet	32 of 35

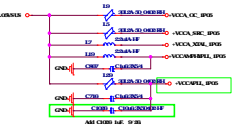




GPIO Group Summary

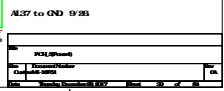
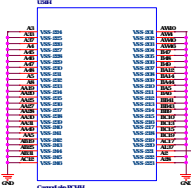
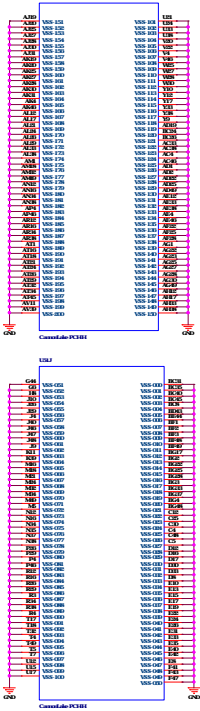
GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCGPPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCGPPFF	1.8V or 3.3V
Primary Well Group G (GPP_G)	VCCGPPG, SPI_0F, VCCGPPG_LPS	1.8V or 3.3V
Primary Well Group H (GPP_H)	VCCGPPH	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCGPPH_LPS	1.8V or 3.3V
Primary Well Group J (GPP_J)	VCCGPPJ	1.8V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

Note: Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage selection soft trip to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft trip only.

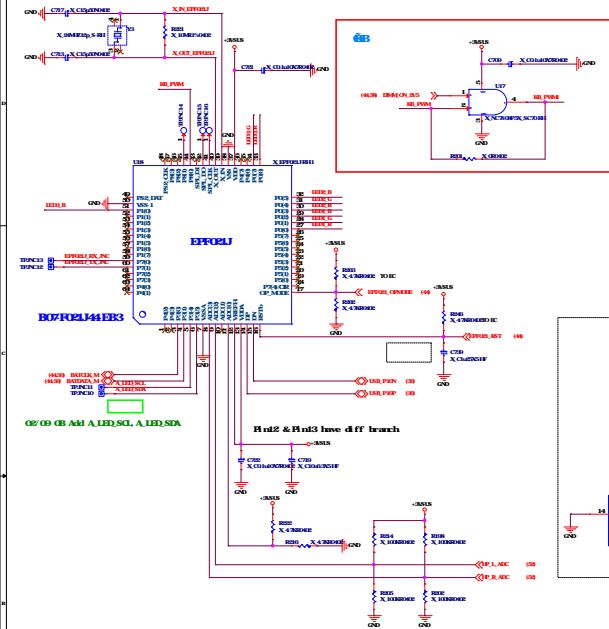


Power Descriptions for PCH in CNL-H

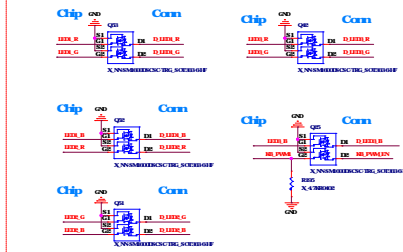
Name	Description
VCCA_BCLK_1P05	Analog supply for BCLK circuitries: 1.05V
VCCA_SRC_1P05	Analog supply for PCIe clock circuitries: 1.05V
VCCA_XTAL_1P05	Analog supply for XTAL circuitries: 1.05V
VCCDUSB_1P05	Supply for USB digital logic: 1.05V
VCCAPLL_1P05	Analog supply for BCLK/DH/ Audio PLLs: 1.05V. This rail can be derived from the VCCPRIM_1P05 rail with the proper isolation. Refer to the Platform Design Guide for implementation detail.
VCCPRIM_1P05	Primary Well: 1.05V. For PCIe/USB/SATA MPHY logic, I/O blocks, SRAM, ITAG, CRV.
VCCDSW_1P05	Deep Sleep Well: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board.
VCCPRIM_MPHY_1P05	Mod PHY Primary: 1.05V. Primary supply for PCIe/USB/SATA MPHY logic and PCI/USB PLL dividers.
VCCANPHYPLL_1P05	Analog supply for USB3, PCIe Gen 2/Gen 3, and SATA3 PLLs: 1.05V. Refer to the Platform Design Guide for filtering and decoupling recommendations.
VCCPRIM_3P3	3.3V Primary Well.
VCCSPI	SPI Primary Well.
VCCSDA	I2C Primary Well.
VCCDSW_3P3	3.3V Deep Sleep Well.
VCCRTC	RTC Well Supply. This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained. Note: VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. Refer to the Platform Design Guide, RTC Design Guidelines chapter for latest design recommendations. Note: Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
DCPRTC	RTC decoupling capacitor only. This rail should NOT be driven.
VCCDPHY_1P24	1.24V for CNV logic. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SOC. Refer to the Platform Design Guide for implementation details.
VCCDPHY_EC_1P24	For decoupling capacitor only. This rail should NOT be driven from the motherboard. This rail can optionally be connected to VCCDPHY_1P24 on the motherboard.
VCCPHVLD0_1P8	1.8V Primary Well. On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCGPPA	1.8V or 3.3V for GPP_A group.
VCCGPPB	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCGPPD	1.8V or 3.3V for GPP_D group.
VCCGPPPE	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCGPPG_3P3	3.3V for GPP_G group.
VCCGPPH	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCMPHY_SENSE	1.05V Sense Line.
VSSMPHY_SENSE	0V (Ground) Sense Line.
VSS	Ground.



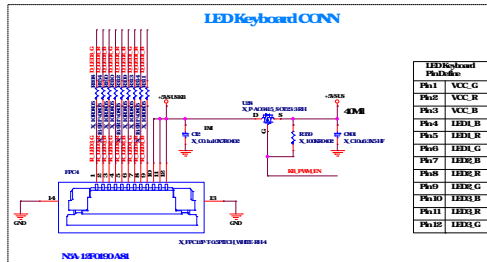
LED8051 Controller



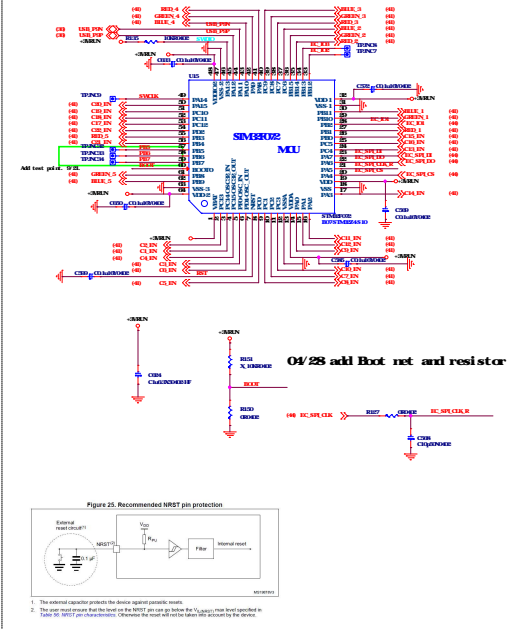
EPRO2U Sink current not enough, only using BSS138(0.22A)



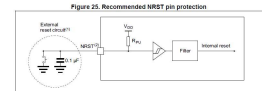
LEDKeyboard CONN



LEDSTM32F02 Controller

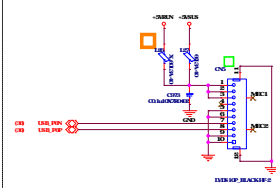


04/28 add Boot net and resistor



1. The external resistor protects the device against possible faults.
2. The user must ensure that the reset pin is pulled up to V_{DD} by a resistor that is not less than 10k.

A side LED

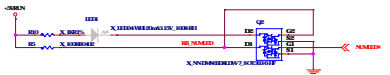


OPSLUED Add LEDB for 17'



LEDB LEDB	
GE	DC 04C3D0 L05
GP	DC 04C3D0 L05

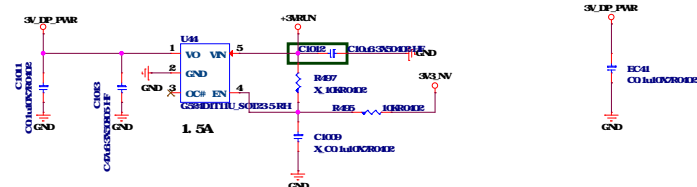
NMLED



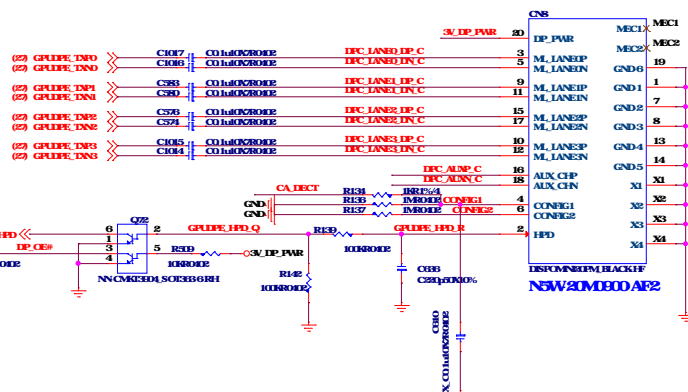
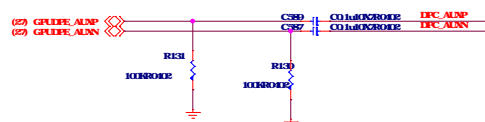
REV: 1.0	DATE: 2017-01-17
DESIGNER: [Name]	CHECKER: [Name]
DATE: 2017-01-17	DATE: 2017-01-17

Display Port

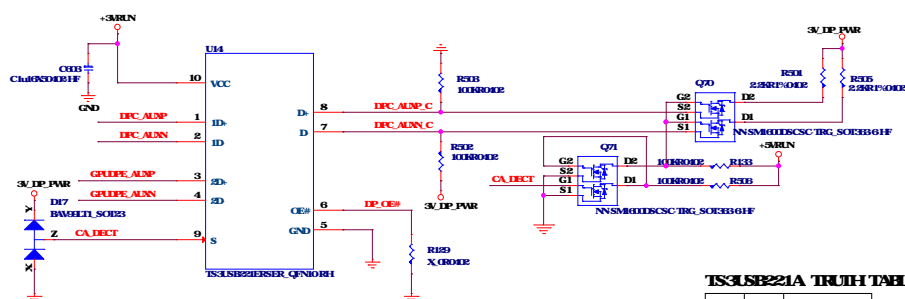
The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin



Display Port



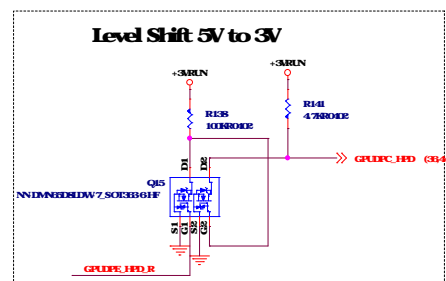
DP/TMS mode select

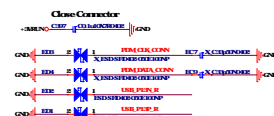
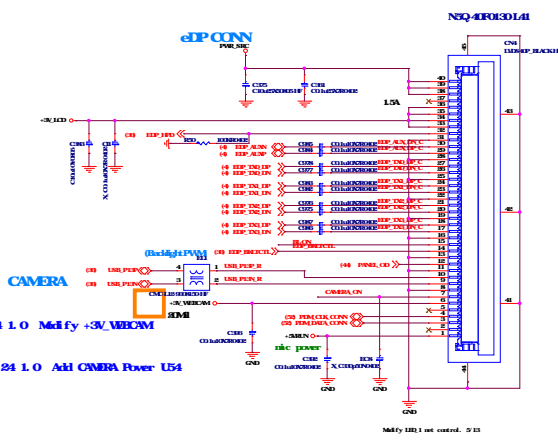
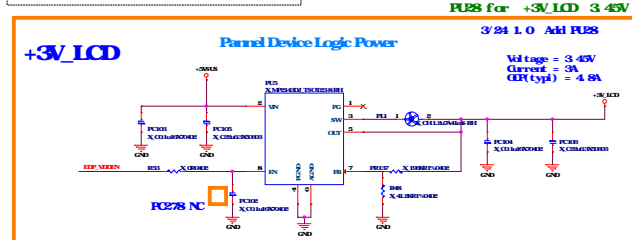
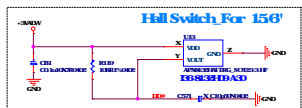
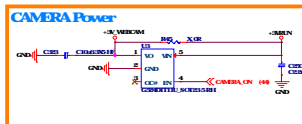
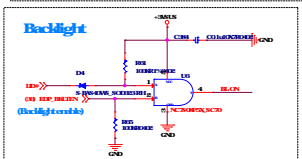
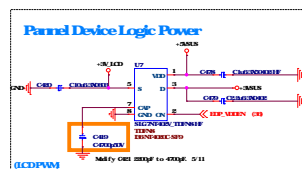


TS3USB221A TRUTH TABLE

S	CE#	FUNCTION
X	H	Il sconnect
L	L	D = 1D
H	L	D = 2D

Level Shift 5V to 3V





LCD Module Pin Define FOR FULL HD PANEL

Pin No	Symbol	Description
1	VDDA	VDDA: VDD
2	H/GND	HighSpeed Ground
3	LANE_N	Complement Signal Lane 1
4	LANE_P	True Signal Lane 1
5	H/GND	HighSpeed Ground
6	LANE_N	Complement Signal Lane 0
7	LANE_P	True Signal Lane 0
8	H/GND	HighSpeed Ground
9	ALN	True Signal Auxiliary Channel
10	ALN	Complement Signal Auxiliary Channel
11	H/GND	HighSpeed Ground
12	ICD_VCC	Power Supply +3.3V (typical)
13	ICD_VCC	Power Supply +3.3V (typical)
14	NC	No Connection (Reserved for CM)
15	H/GND	Ground
16	H/GND	Ground
17	H/D	H/D Pin Detect
18	H_GND	H_GND
19	H_GND	H_GND
20	H_GND	H_GND
21	H_GND	H_GND
22	H_IN	H_Inhibit Signal of LED Connector
23	H_PWM	PWM Dimming Control Signal of LED Connector
24	VDDA	VDDA: VDD
25	NC	No Connection (Reserved)
26	LED_VCCS	LED Power
27	LED_VCCS	LED Power
28	LED_VCCS	LED Power
29	LED_VCCS	LED Power
30	OE_IN	OE Inhibit Signal of ICN

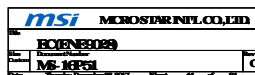
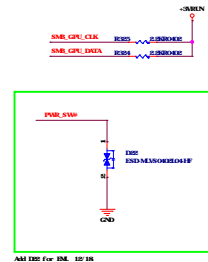
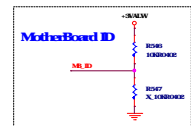
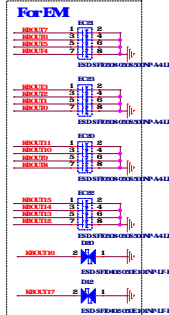
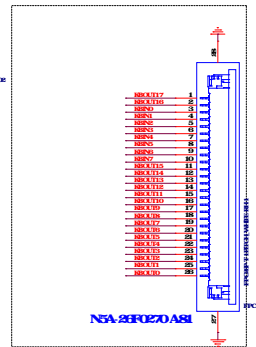
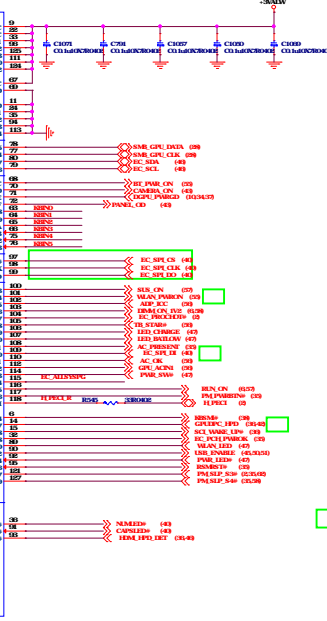
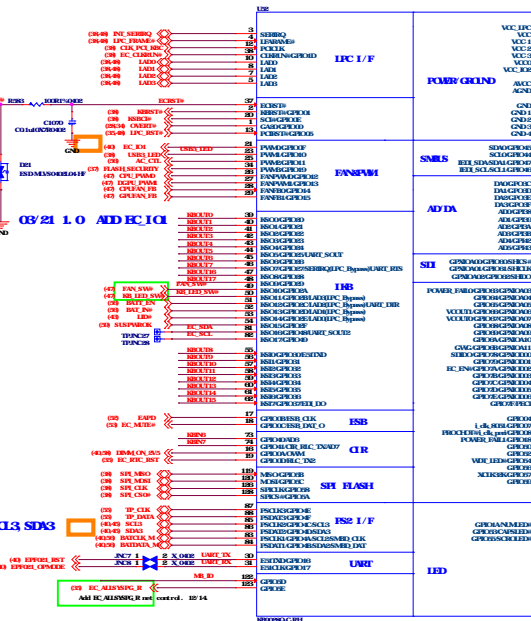
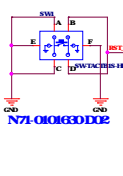
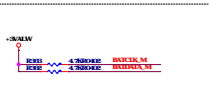
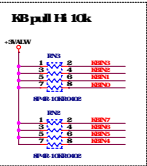
LCD Module Pin Define FOR WQHD PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H/GND	HighSpeed Ground
3	LANE_N	Complement Signal Lane 3
4	LANE_P	True Signal Lane 3
5	H/GND	HighSpeed Ground
6	LANE_N	Complement Signal Lane 2
7	LANE_P	True Signal Lane 2
8	H/GND	HighSpeed Ground
9	LANE_N	Complement Signal Lane 1
10	LANE_P	True Signal Lane 1
11	H/GND	HighSpeed Ground
12	LANE_P	True Signal Lane 0
13	LANE_N	Complement Signal Lane 0
14	H/GND	HighSpeed Ground
15	ALN	True Signal Auxiliary Channel
16	ALN	Complement Signal Auxiliary Channel
17	H/GND	HighSpeed Ground
18	VED	LED logic and driver power (3.3V)
19	VED	LED logic and driver power (3.3V)
20	VED	LED logic and driver power (3.3V)
21	VED	LED logic and driver power (3.3V)
22	HST	HST (HDMI) pin
23	H_GND	H_GND
24	H_GND	H_GND
25	H_GND	H_GND
26	H_GND	H_GND
27	H_GND	H_GND
28	H_GND	H_GND
29	H_GND	H_GND
30	OE_IN	OE Inhibit Signal of ICN

KBC/EC/P (ENE9123)

Hardware Reset

PUPD



USB3.1 TYPE C ASML532 Re-timer

USB3.1 Gen2 Retimer

Strap

+1.2ASUS

MAX1A

ESD

ASML533 Mix with CCL

Function Table

Function	Pin	Signal
Power	1	VBUS
Ground	2	GND
NC	3	NC
NC	4	NC
NC	5	NC
NC	6	NC
NC	7	NC
NC	8	NC
NC	9	NC
NC	10	NC
NC	11	NC
NC	12	NC
NC	13	NC
NC	14	NC
NC	15	NC
NC	16	NC
NC	17	NC
NC	18	NC
NC	19	NC
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NC	89	NC
NC	90	NC
NC	91	NC
NC	92	NC
NC	93	NC
NC	94	NC
NC	95	NC
NC	96	NC
NC	97	NC
NC	98	NC
NC	99	NC
NC	100	NC

Strapping Table

Strap	Pin	Signal
Power	1	VBUS
Ground	2	GND
NC	3	NC
NC	4	NC
NC	5	NC
NC	6	NC
NC	7	NC
NC	8	NC
NC	9	NC
NC	10	NC
NC	11	NC
NC	12	NC
NC	13	NC
NC	14	NC
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NC	99	NC
NC	100	NC

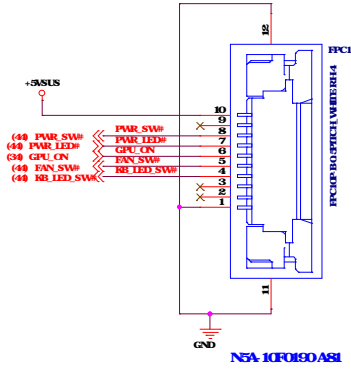
USB20CMC

Type C Connector

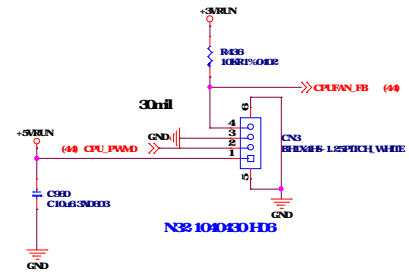
PWR Switch

Rev	1.0
Date	2018/08/01
Author	ASML533
Checker	ASML533
Version	1.0
Page	1 of 1

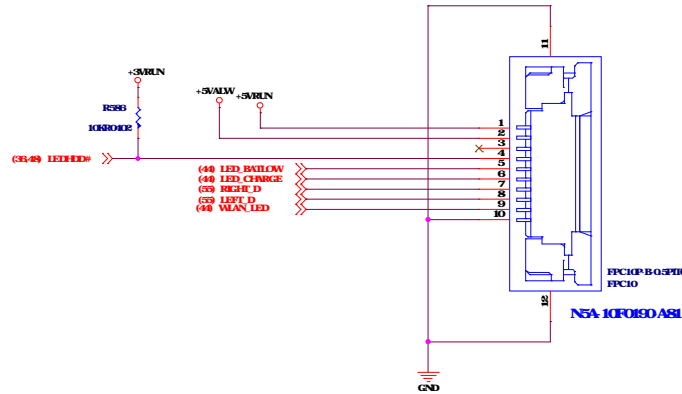
Power Switch Connector



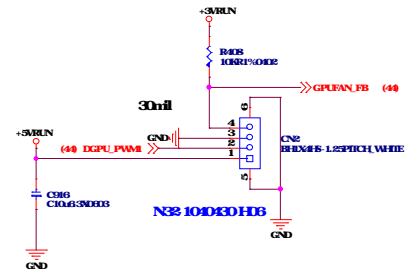
CPU FAN



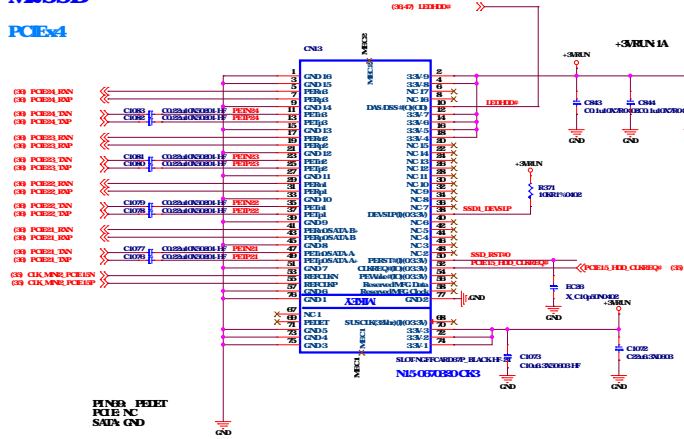
Switch connector



DGPU FAN

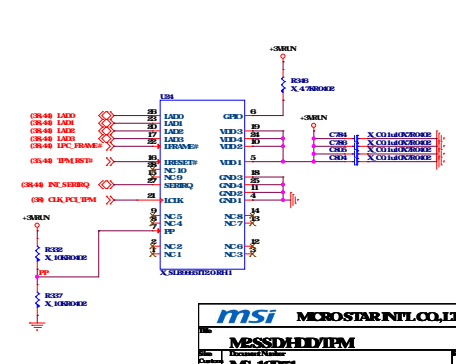
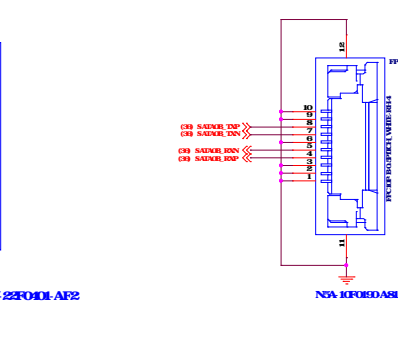
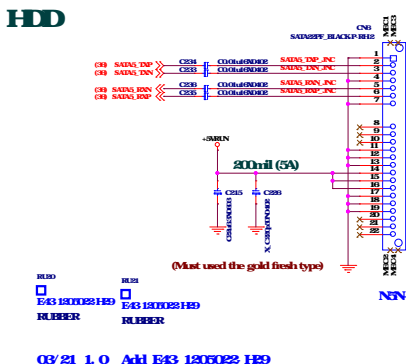
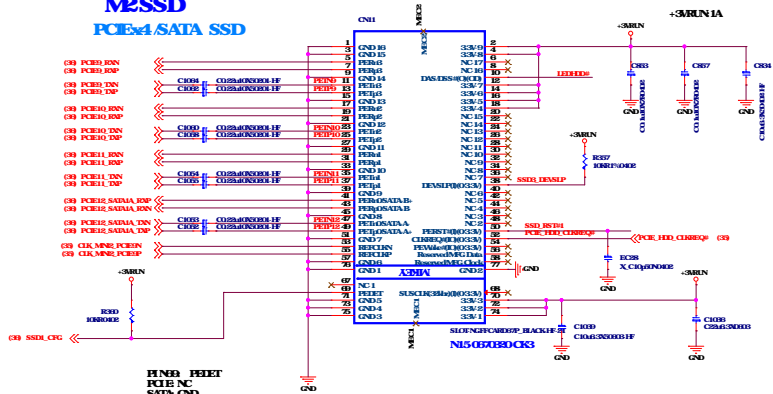
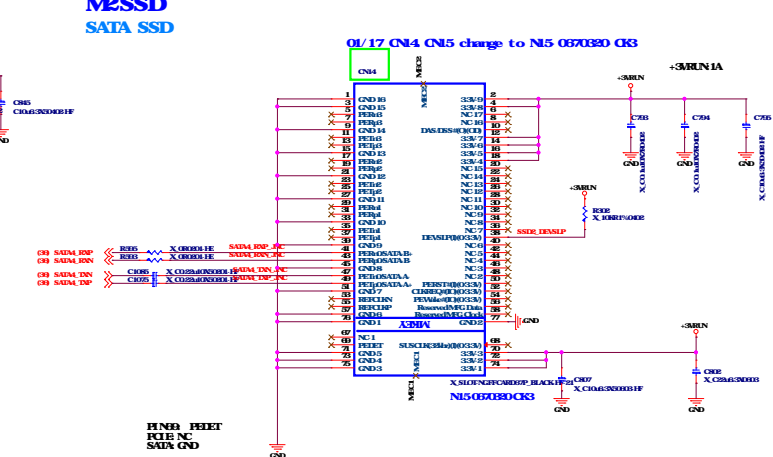
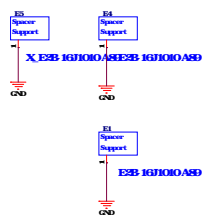


msi MICROSTAR INT'L CO., LTD.	
File	CPU FAN B1B CONN LED
Docu	Document Number
Custom	MS-16P51
Date	Thursday, December 28, 2006
Sheet	47 of 84
Rev	0A




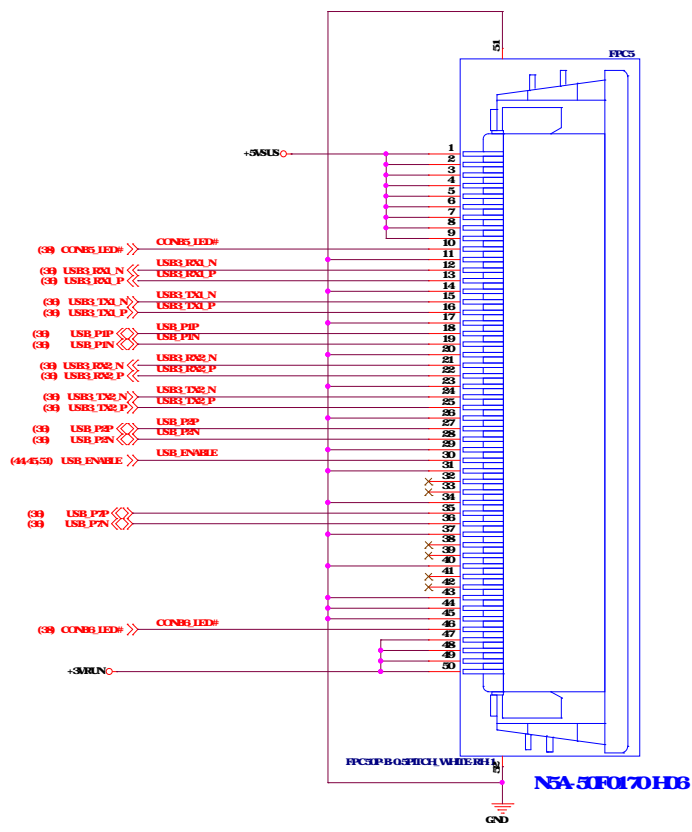
SSD_BTH0
SSD_BTH1

40	NC	No Connect
41	SATA-B-/PERnD	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERpD	Host receiver differential signal pair
44	GND	Ground
45	NC	No Connect
46	NC	No Connect
47	SATA-A-/PETH	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A-/PETpD	Host transmitter differential signal pair



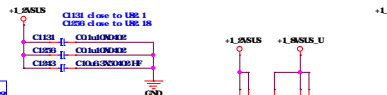
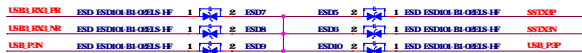


		MICROSTAR INT'L CO., LTD.	
Title			
Giga LAN (E250)			
Site	Document Number	Rev	
Customer	MS-16P51	0A	
Dates	Thursday, December 28, 2007	Sheet	49 of 84

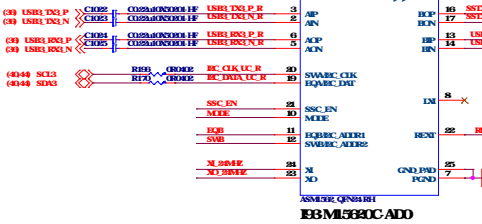


		MICROSTAR INT'L CO., LTD.	
Title			
USB 30connector			
Size	Document Number		Rev
Custom	MS-16P51		0A
Date	Thursday, December 28, 2017	Sheet	50 of 84

USB 31 CNT3

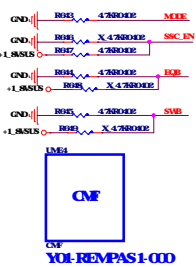


USB31 Gen2 Retimer



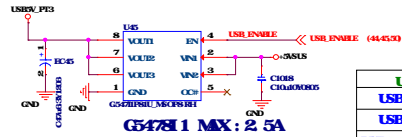
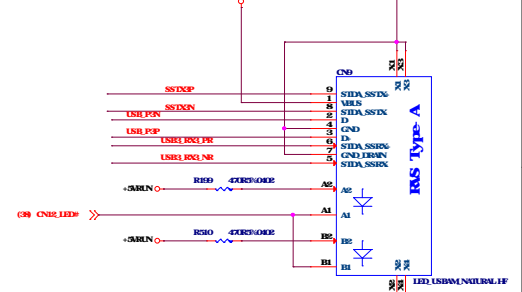
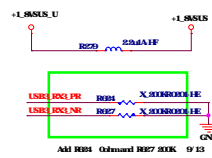
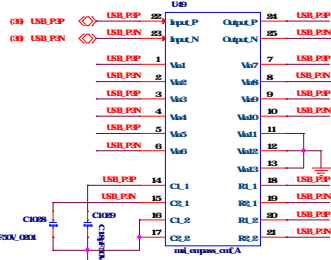
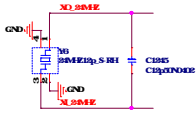
EBM1580C-AD0

Strap



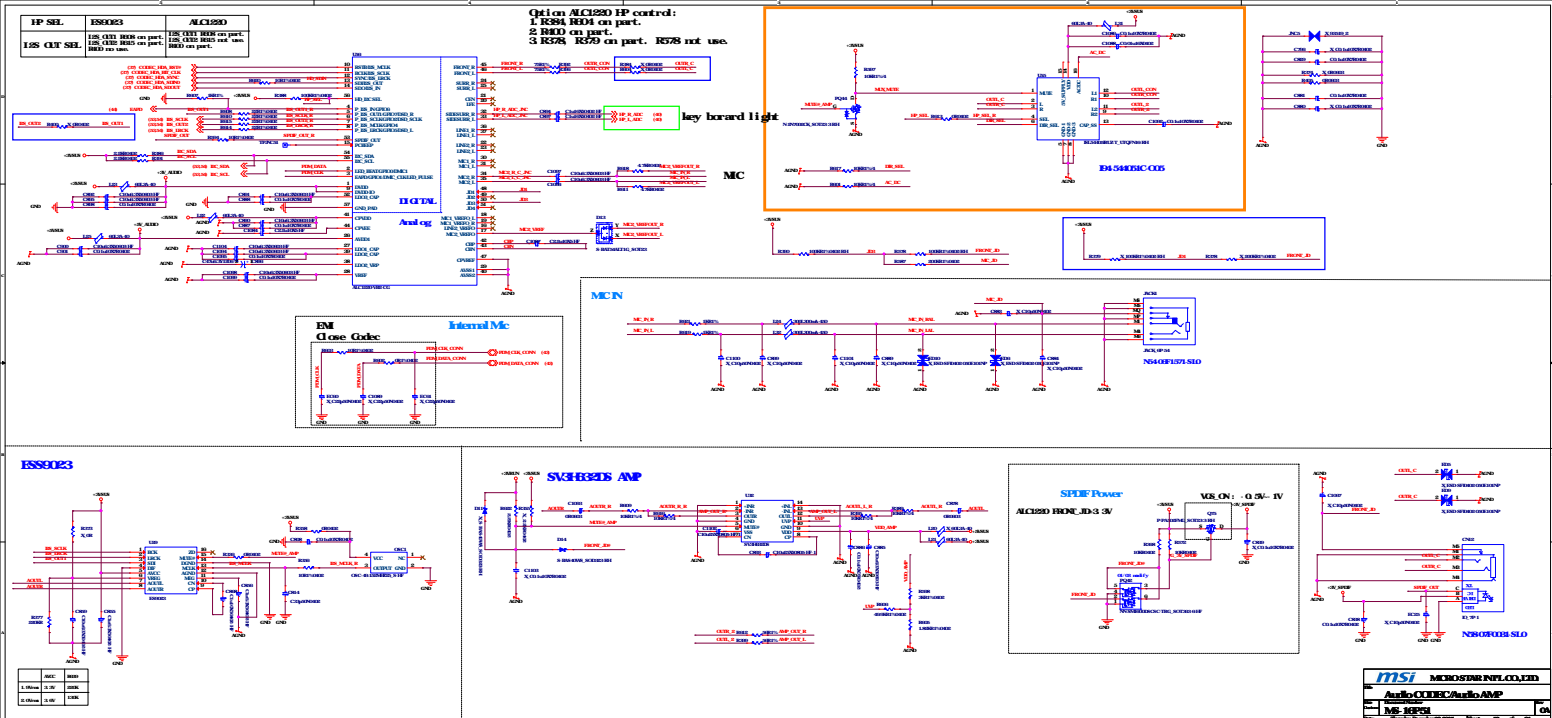
MCE: mode select
H: ATE Test mode
M: Stopping mode
L: EC mode (v)
SSC_EN: Speed/Spectrum
H: SSC enable
L: SSC disable (v)
EC_Male: EC Address
EQ0 = Address 1; SWB = Address 2
IL = 75

24MHz Clock



USB3_0	N33 03M031-AF2
USB3_0_LED	N33 13M031-LO3
USB3_1_GEN2	N33 03M021-AF2
USB3_1_GEN2_LED	N33 13M021-LO3

msi MICROSTAR INT'L CO., LTD	
USB 31 connector	
Doc No:	MS-10P21
Date:	Revised December 28, 2007



0V/07 L.O C866 C797 change to C71-150251G S03

HBDD
Active low to shutdown /MP (L= shutdown ; H= normal)

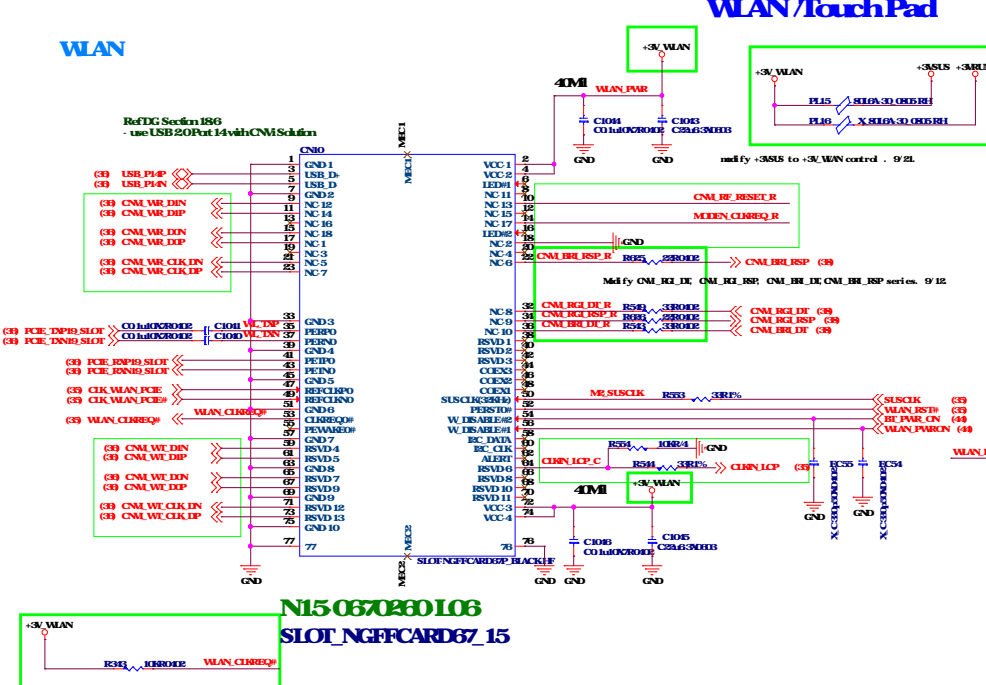
I2C address selection (L= 0x0H; H= 0x2H)

AIC303

WLAN/TouchPad

WLAN

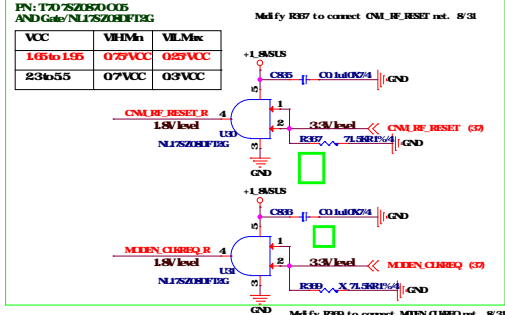
Ref DG Section B86
- use USB 2.0 Port 14 with CN1 Solution



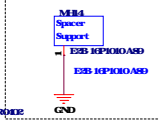
N15 0670280 L06
SLOT_NGFFCARD67_15

PN: T702S080005
AND Gate/NL7SZ0HFBT

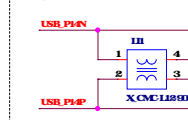
VCC	VHMin	VHMax
1.65 to 1.95	0.7VCC	0.8VCC
2.3 to 5.5	0.7VCC	0.9VCC



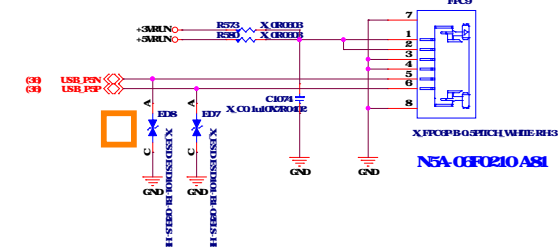
WLANStand off



EM



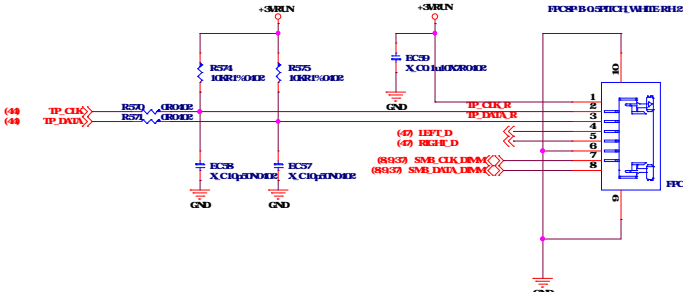
FP



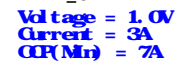
TouchPad

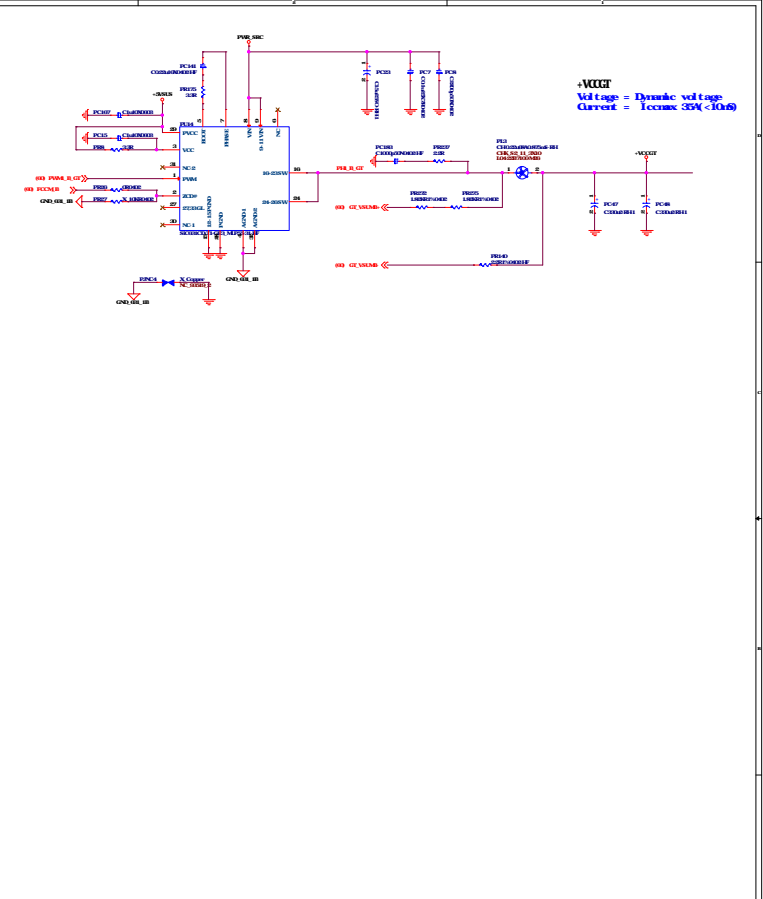
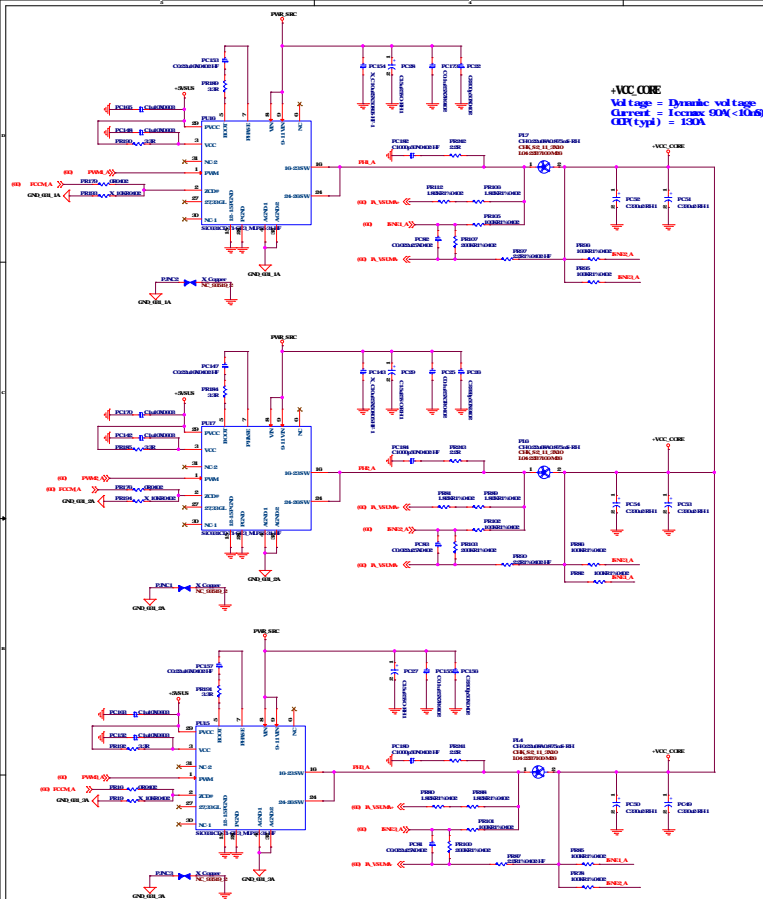
03/20 FPC12 change to N5A 08F0130 H03

N5A 08F0130 H03

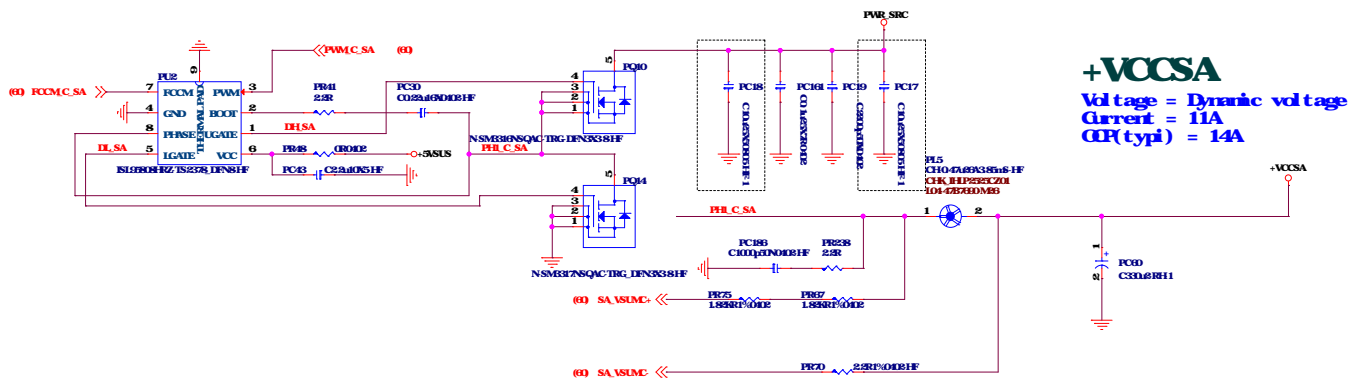


Voltage = 1.8V
Current = 4A
OCP(Min) = 7A

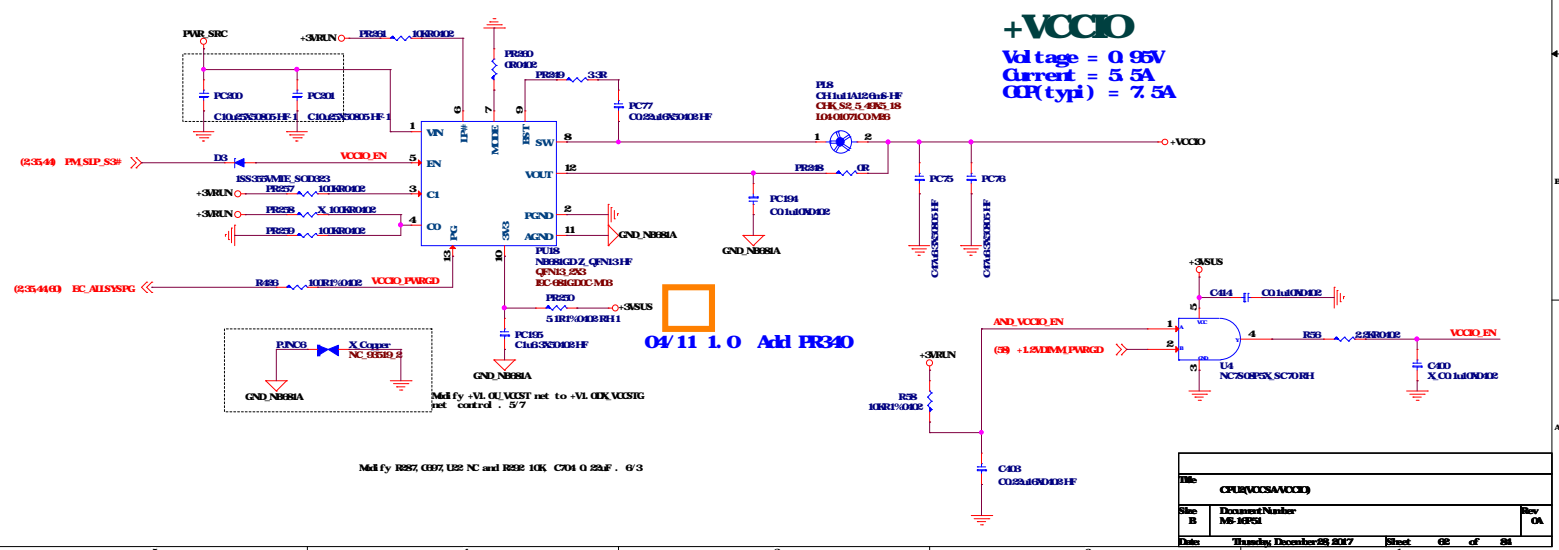




NO	DESCRIPTION	UNIT
1	PCAP	PCAP
2	VIA	VIA
3	TRAIL	TRAIL



+VCCSA
 Vol tage = Dynamic vol tage
 Current = 11A
 QP (typi) = 14A

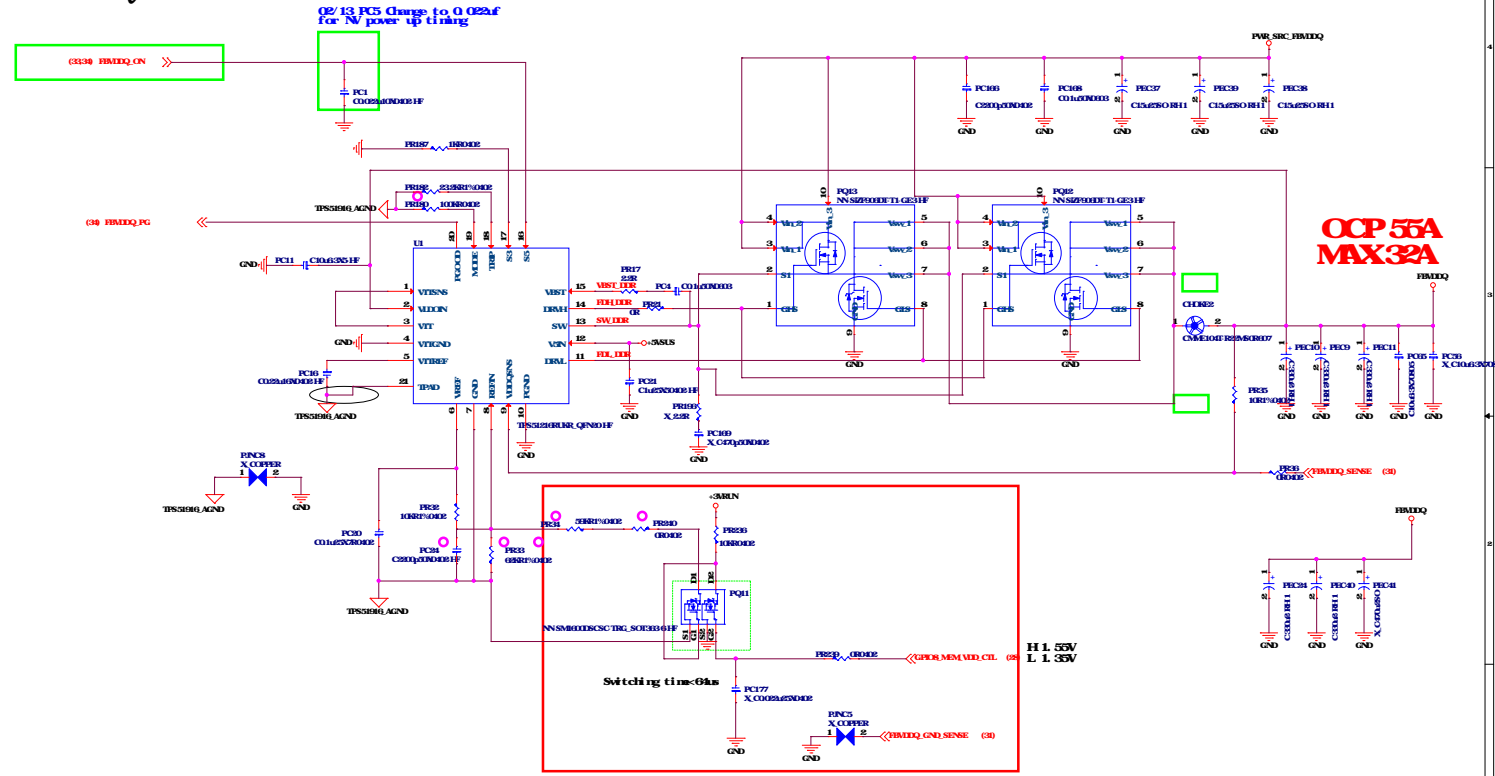



+VCCIO
 Vol tage = 0.95V
 Current = 5.5A
 QP (typi) = 7.5A

04/11 1.0 Add PR340

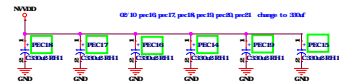
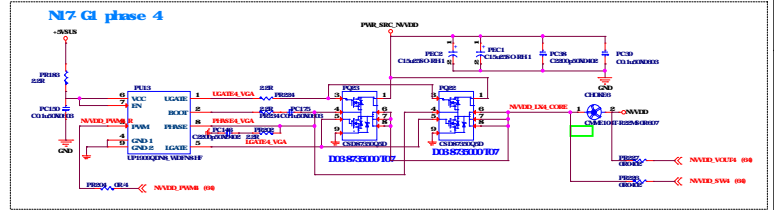
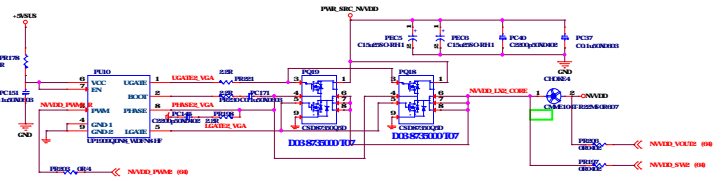
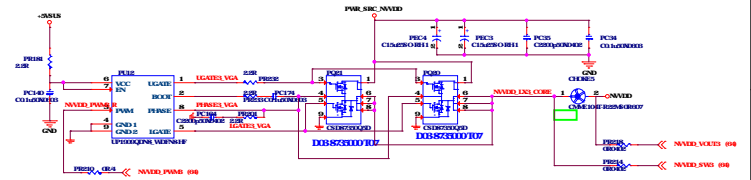
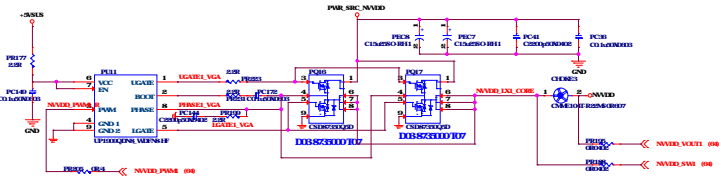
Modfy B287, C107, U25 NC and B282 10K C104 0.22uF . 0/3

Title		
CPU(VCCSA/VCCIO)		
Sheet	Document Number	Rev
1	M5-10F01	0A
Date	Thursday, December 28, 2007	Sheet 02 of 04

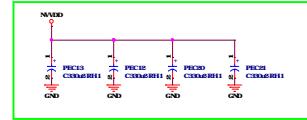


		MICROSTAR INT'L CO., LTD.	
Title: DGPU POWER FBVDDQ			
Doc. No.	Document Number		Rev
	MS-1GP51		0A
Date	Sheet	03	of 03

DGPU POWER
EDP Peak 300A
EDP Con 115A



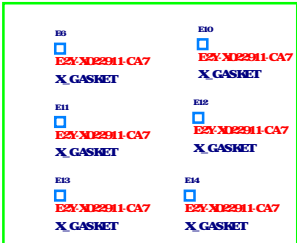
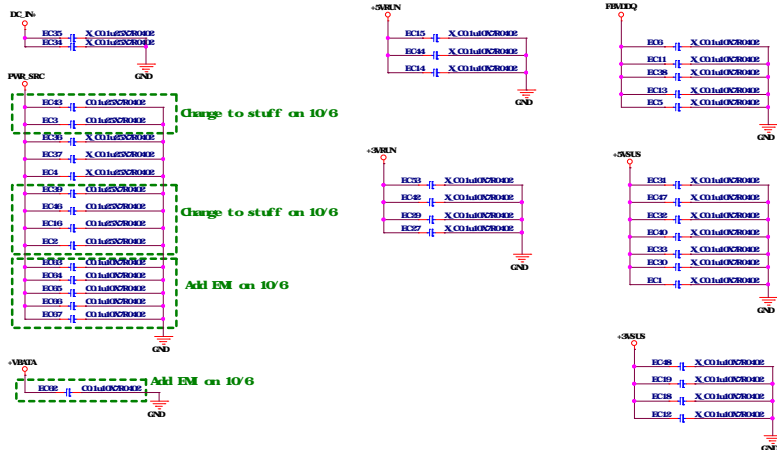
2016/12/28 N7-G1 CB Add 330uF for N7-G1



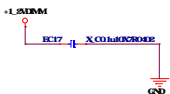
N7-G1

PC12	NC
PC13	NC

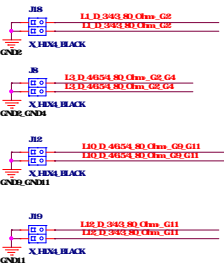
Rev	001
By	001
Check	001
Date	2016/12/28



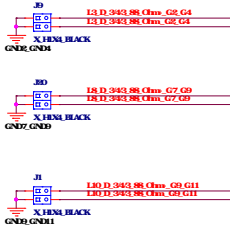
Add E4, E5, E6, E7, E8, E9 for EML 5/22



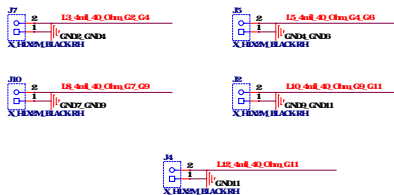
80 OHM / CLK/WCK/USB3.1



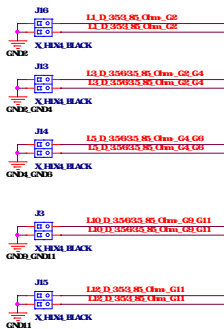
88 OHM / DDR4 CLK



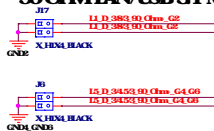
40 OHM / DDR4 CTRL



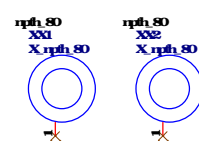
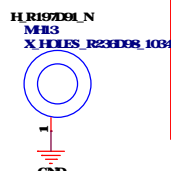
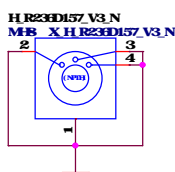
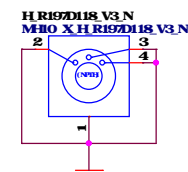
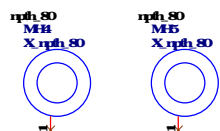
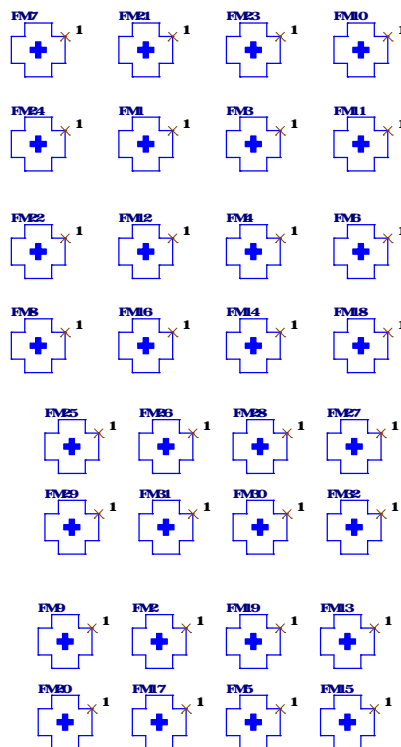
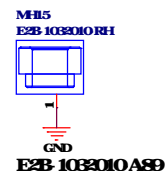
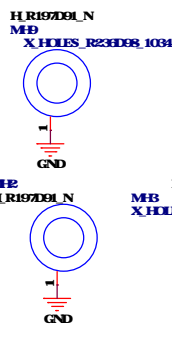
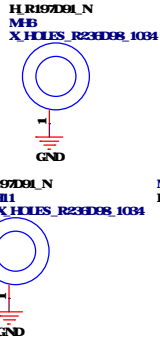
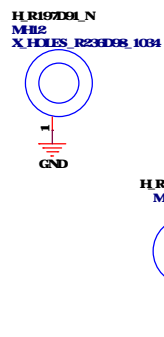
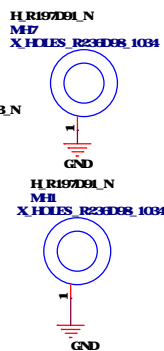
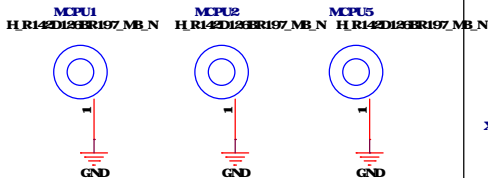
85 OHM / SATA / PCH/PCIE / HDP USB / HDM/DP/DM/CLK/PEG



90 OHM LAN/USB3.1 MUX



CPU Holes



160629



3076P10111-HG0



3076P10211-HG0



E2P-4A11411-Y42



E2P-4A11011-Y42



E2P-6P11311-Y42



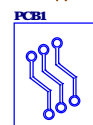
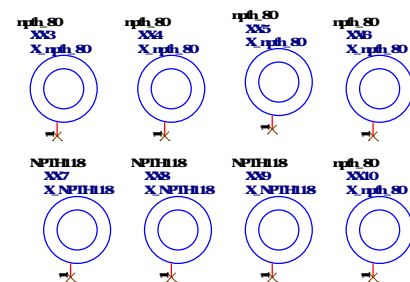
E2P-6P11311-Y42



E2P-6P11311-Y42



E2P-6P11311-Y42



PDO 16P5110H73

Humstar: PDO 16P5110 H73
TRIPD PDO 16P5110 T53



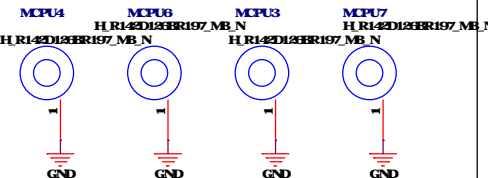
HM00000000 G51-NICO001-A09

For MP



HCS_LABEL

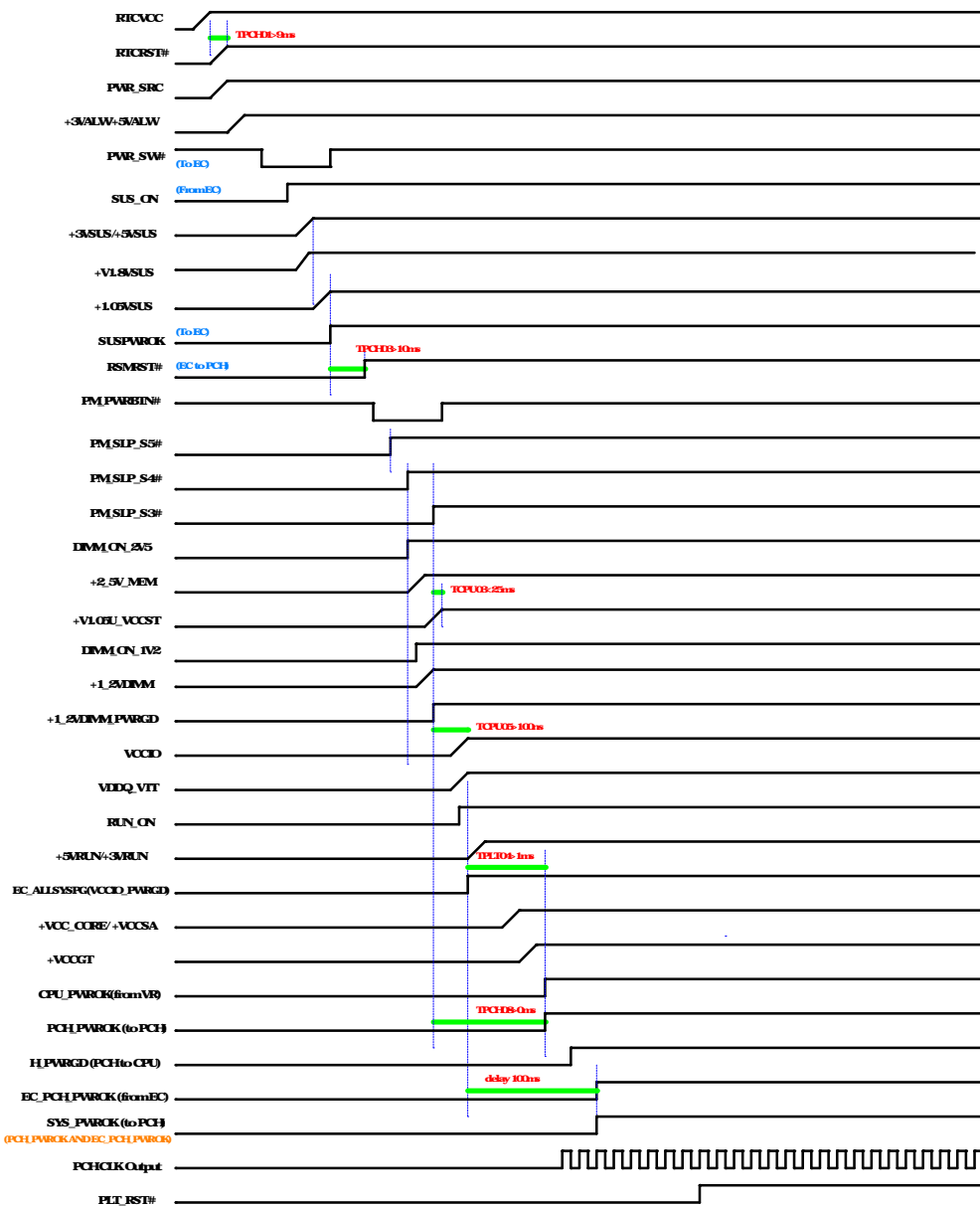
DGPU Holes



msi MICROSTAR INT'L CO., LTD.			
Title	ScrewME		
Doc Number	MS-16P51		
Customer	M6-16P51		
Date	Thursday, December 28, 2017	Sheet	06 of 84

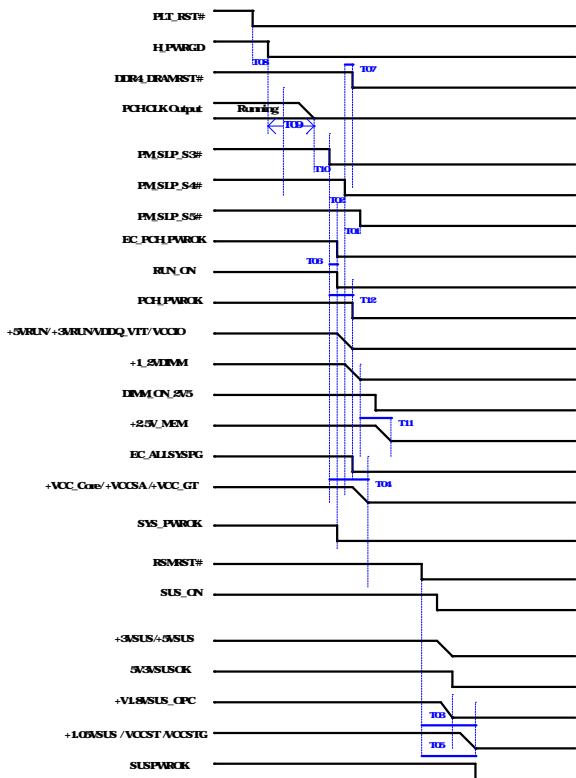
Power on Sequence

G3 -> S0



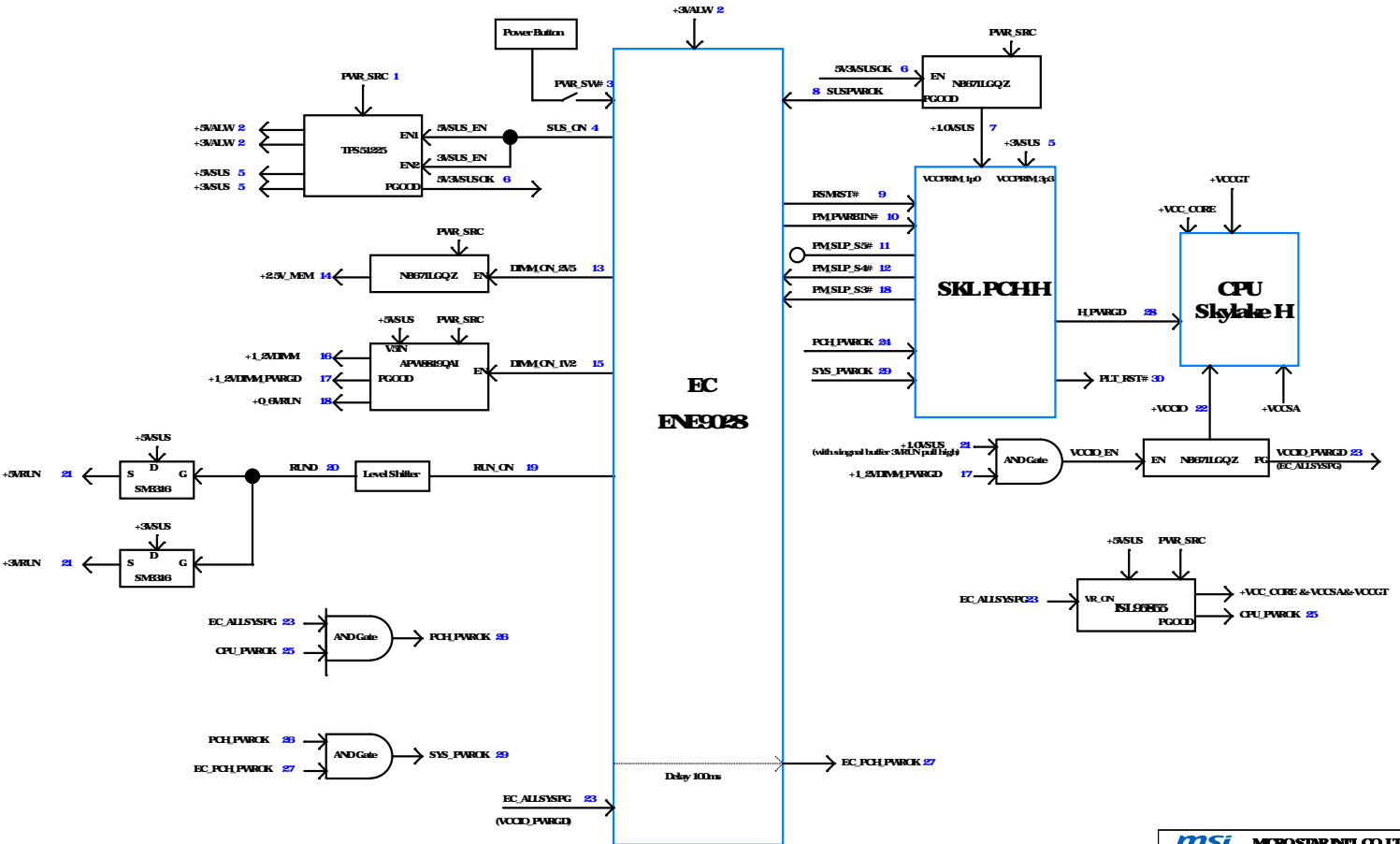
Power down Sequence

S0-> G3



	MN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMST# asserting to VccPRM drooping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off
T05	1		us	RSMST# asserting to VccPRM drooping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD deassertion to CLKOUT_BCLK turning OFF
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWRCK deassertion

MS-16P1 Power on Block Diagram



History

OB:

2017/08/31

1. Modify R367 to connect CNM_R#_RESET net. Page 55
2. Modify R369 to connect MDEN_CLKREQ net. Page 55
3. Modify R515, R516 change 0 22uF. Page 51

2017/09/7

1. Modify C738, C734, C730, C724 0 1uF to 0 22uF. page 45
2. Modify R275, R539. Ohmard R552, R538 no use. page45
3. Modify R196. Ohmard R170 no use. page 51.

2017/09/12

1. Modify SPI_MISO, SPI_MOSI, SPI_CS0#, SPI_CLK series 33R. page 38
2. Modify CNM_RQ_DE, CNM_RQ_RSP, CNM_RR_DE, CNM_RR_RSP series. page 55

2017/09/13

1. Add R824. Ohmard R827 200K. page 51
2. PR158, PR159 33 2K(R11-3322T12 V01). page 57.
3. PR121 => 3 92ohmfor L.L. (R11-3321U12 V09). page 60
4. PR138 => 78 7ohmfor IMDN (R11-7872U12 V09). page 60
5. PC89 => 82uF for RC match (C11-8232512 V01). page 60
6. PR270 => 1 82ohmfor LL(R11-1821T12 R01). page 60
7. PC92 => 0 047uF for RC match(C11-4732312 V09). page 60
8. PR136 => 5 43ohm(R11-5491T12 R01). page 60
9. PR139 => 105ohmfor IMDN(R11-1053T12 R01). page 60
10. Add C1107, C1108, C1108 22uF. page 7.

2017/09/18

1. Add U81 32MBH1G8 RAMfor Wicestation use. page 38
2. R90 change 6 98K ohmpage 46

2017/09/21

1. Add R598 0 ohm. page 35
2. Modify EC_FCH_PWMCK. page 35
3. Remove U83. page 35
4. modify +3VSUS to +3V_VI/AN control. page 55
5. Add test point. page 40
6. Add C1109, C1110, C1111, C1112 22uF. page 45, 51.
7. Add C1088 1uF. page 39.
8. Remove TRNG test pin. page3
9. Add C1114, C1113, C1115 22uF. page 7.

2017/09/22

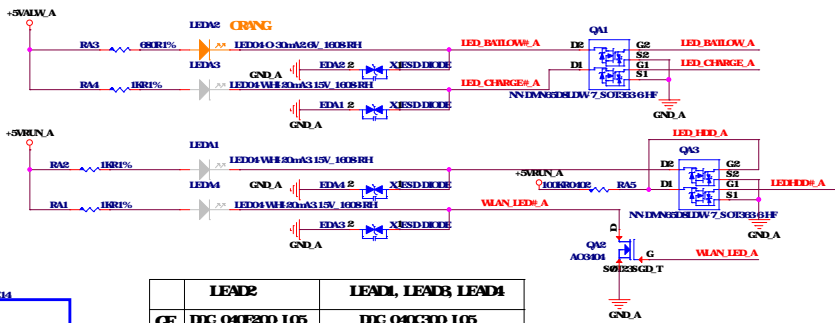
1. change PR128 450ohmto 249 ohm. page 60
2. change PR129 2 94K to 1.82 K. page 60
3. Change PC98 1000uF to 680uF. page 60

2017/09/25

1. change R275, R552 footprint 0603
2. change R196, R170 footprint 0603
3. change R258, R251, R231, R238 200K 0801.

2017/09/26

1. QFP_R21 add R637 10K ohm
2. Change C731, C727, C741, C737, C744, C742, C729, C723 to 0 33uF.
3. Modify R515, R516 change 0 33uF.



	LEAD2	LEAD1, LEAD3, LEAD4
GE	DDC 040B200 L05	DDC 040C300 L05
GP	DDC 040B80 L05	DDC 040B010 L05

U1E4
NE
MLAR

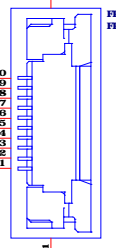
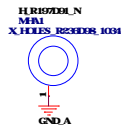
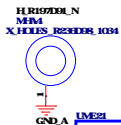
POWER ADHESIVE
E2X-6P11111-Y42

16
GE E2X 6P11111-Y42 on part.
GP E2X 6P11111-Y42 no use. 9/14

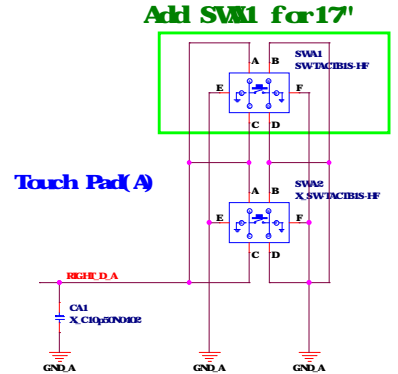


PDD 16P5A10H23

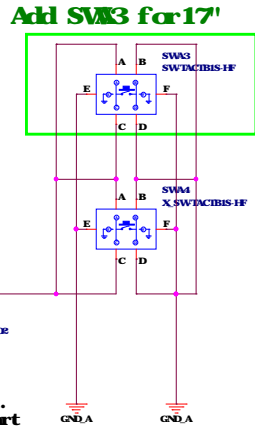
Hinestar: PDD 16P5A10 H23
TRIPD PDD 16P5A10 T53



NSA 10P080A81



17" SW1 on part.
15 6" SW2 on part



17" SW3 on part.
15 6" SW4 on part

msi MICROSTAR INT'L CO., LTD

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History

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<div><div><div>msi</div><div>MCROSTAR INT'L CO., LTD</div></div></div>		
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[A]History		
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G547E1 MAX : 2 5A

USB0_0	NES 06M008L AP2
USB0_0_LED	NES 13M003L L03
USB0_1_GEN2	NES 06M001 AP2
USB0_1_GEN2_LED	NES 13M001L L03

[illegible]

The diagram illustrates the internal circuitry of the G54781 MX:2 5A RAS Type-A module. Key components include a transformer (T1) for power conversion, a bridge rectifier (BR1) for AC-to-DC conversion, and various capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100) for filtering and timing. The module is connected to a USB_PSP.B signal line, which is split into USB_PSN.B and USB_PSP.B. The USB_ENABLE.B and USB_ENABLE_N.B signals are also shown. The module is labeled "RAS Type-A" and "G54781 MX:2 5A".

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G54781-MX-2-5A	1.0	1.0

Table 1. Pin Definitions

Pin	Signal	Function
1	USB_PSP.B	USB Power Sense
2	USB_PSN.B	USB Power Sense
3	USB_ENABLE.B	USB Enable
4	USB_ENABLE_N.B	USB Enable
5	USB_PSP.B	USB Power Sense
6	USB_PSN.B	USB Power Sense
7	USB_ENABLE.B	USB Enable
8	USB_ENABLE_N.B	USB Enable
9	USB_PSP.B	USB Power Sense
10	USB_PSN.B	USB Power Sense
11	USB_ENABLE.B	USB Enable
12	USB_ENABLE_N.B	USB Enable
13	USB_PSP.B	USB Power Sense
14	USB_PSN.B	USB Power Sense
15	USB_ENABLE.B	USB Enable
16	USB_ENABLE_N.B	USB Enable
17	USB_PSP.B	USB Power Sense
18	USB_PSN.B	USB Power Sense
19	USB_ENABLE.B	USB Enable
20	USB_ENABLE_N.B	USB Enable
21	USB_PSP.B	USB Power Sense
22	USB_PSN.B	USB Power Sense
23	USB_ENABLE.B	USB Enable
24	USB_ENABLE_N.B	USB Enable
25	USB_PSP.B	USB Power Sense
26	USB_PSN.B	USB Power Sense
27	USB_ENABLE.B	USB Enable
28	USB_ENABLE_N.B	USB Enable
29	USB_PSP.B	USB Power Sense
30	USB_PSN.B	USB Power Sense
31	USB_ENABLE.B	USB Enable
32	USB_ENABLE_N.B	USB Enable
33	USB_PSP.B	USB Power Sense
34	USB_PSN.B	USB Power Sense
35	USB_ENABLE.B	USB Enable
36	USB_ENABLE_N.B	USB Enable
37	USB_PSP.B	USB Power Sense
38	USB_PSN.B	USB Power Sense
39	USB_ENABLE.B	USB Enable
40	USB_ENABLE_N.B	USB Enable
41	USB_PSP.B	USB Power Sense
42	USB_PSN.B	USB Power Sense
43	USB_ENABLE.B	USB Enable
44	USB_ENABLE_N.B	USB Enable
45	USB_PSP.B	USB Power Sense
46	USB_PSN.B	USB Power Sense
47	USB_ENABLE.B	USB Enable
48	USB_ENABLE_N.B	USB Enable
49	USB_PSP.B	USB Power Sense
50	USB_PSN.B	USB Power Sense
51	USB_ENABLE.B	USB Enable
52	USB_ENABLE_N.B	USB Enable
53	USB_PSP.B	USB Power Sense
54	USB_PSN.B	USB Power Sense
55	USB_ENABLE.B	USB Enable
56	USB_ENABLE_N.B	USB Enable
57	USB_PSP.B	USB Power Sense
58	USB_PSN.B	USB Power Sense
59	USB_ENABLE.B	USB Enable
60	USB_ENABLE_N.B	USB Enable
61	USB_PSP.B	USB Power Sense
62	USB_PSN.B	USB Power Sense
63	USB_ENABLE.B	USB Enable
64	USB_ENABLE_N.B	USB Enable
65	USB_PSP.B	USB Power Sense
66	USB_PSN.B	USB Power Sense
67	USB_ENABLE.B	USB Enable
68	USB_ENABLE_N.B	USB Enable
69	USB_PSP.B	USB Power Sense
70	USB_PSN.B	USB Power Sense
71	USB_ENABLE.B	USB Enable
72	USB_ENABLE_N.B	USB Enable
73	USB_PSP.B	USB Power Sense
74	USB_PSN.B	USB Power Sense
75	USB_ENABLE.B	USB Enable
76	USB_ENABLE_N.B	USB Enable
77	USB_PSP.B	USB Power Sense
78	USB_PSN.B	USB Power Sense
79	USB_ENABLE.B	USB Enable
80	USB_ENABLE_N.B	USB Enable
81	USB_PSP.B	USB Power Sense
82	USB_PSN.B	USB Power Sense
83	USB_ENABLE.B	USB Enable
84	USB_ENABLE_N.B	USB Enable
85	USB_PSP.B	USB Power Sense
86	USB_PSN.B	USB Power Sense
87	USB_ENABLE.B	USB Enable
88	USB_ENABLE_N.B	USB Enable
89	USB_PSP.B	USB Power Sense
90	USB_PSN.B	USB Power Sense
91	USB_ENABLE.B	USB Enable
92	USB_ENABLE_N.B	USB Enable
93	USB_PSP.B	USB Power Sense
94	USB_PSN.B	USB Power Sense
95	USB_ENABLE.B	USB Enable
96	USB_ENABLE_N.B	USB Enable
97	USB_PSP.B	USB Power Sense
98	USB_PSN.B	USB Power Sense
99	USB_ENABLE.B	USB

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SHERRO			
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2017/8/31

1. Modify RB18, RB19, RB30, RB31 0 22uF. page 77

2017/9/7

1. Modify RB13 Ohmand RB37 no use. page 77.

2017/9/13

1. Add RB38, RB39 200K page 77

2 Add RB40, RB41 200K page 77

2017/9/21

1. modify CB13 47uF. page 76

2 modify CB3 footprint 0805 to 0603 page 76

2017/9/25

1. change RB13 and RB37 footprint 0603 add CB32, CB33 22uF. page 77.

2 modify RB1-RB3 0 ohm. page 76

2017/9/26

1. Add CB34 22 uF and Change CB3 to 22uF.

2 Modify RB18, RB19 change 0 33uF.

3 Modify RB30, RB31 change 0 33uF.

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ICPowerSwitch			
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2017/9/12

1. Modify RC3, RC2, LED2, LED3, QC1, EDC2, EDC3 no use . page 79

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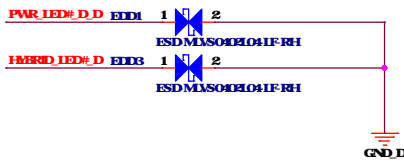
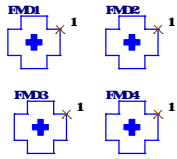
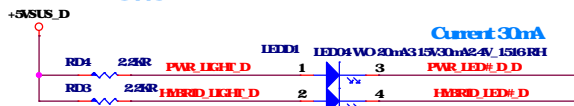
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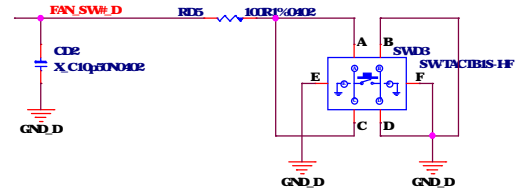
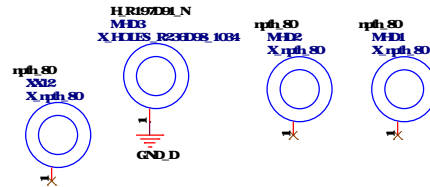
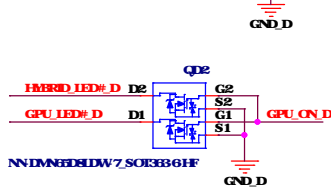
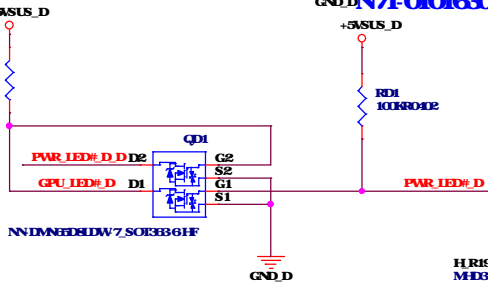
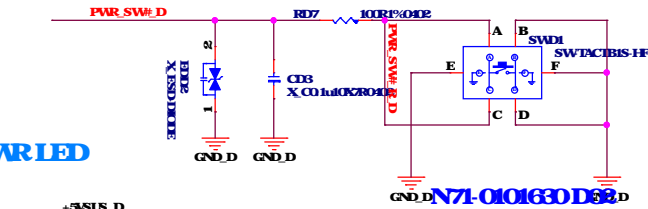
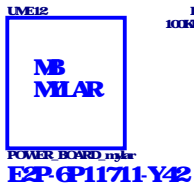
1

PowerLED

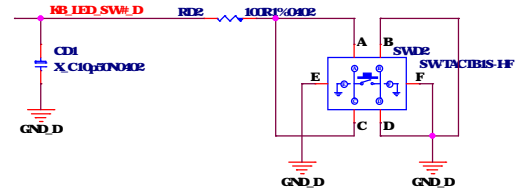


PowerSwitch

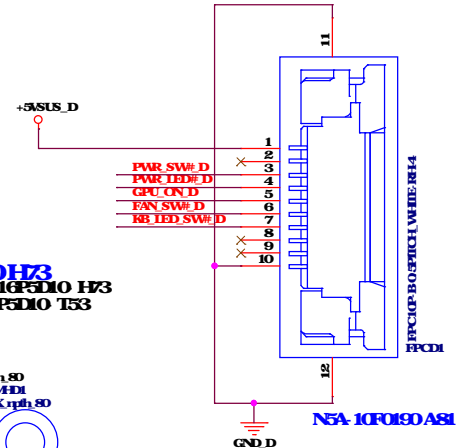
Control PWR LED



N71-0101630 D02



N71-0101630 D02



N5A-10F0180 A81

Title				
PWRPowerSwitch				
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2017/02/06

1. Add MD7, delete MC13

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